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Design and Development of Multilevel Inverter for Solar Power Generation

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Abstract-This paper proposes a solar power generation system is composed of a dc–dc power converter and a seven level inverter. The seven-level inverter contains only six power electronic switches, which simplifies the circuit configuration. Furthermore, only one power electronic switch is switched at high frequency at any time to generate the seven-level output voltage. This reduces the switching power loss and improves the power efficiency and also reduces the Total Harmonic Distortion (THD). The voltages of the two dc capacitors in the proposed seven-level inverter are balanced automatically, so the control circuit is simplified. Simulation results show that the proposed solar power generation system generates a seven-level output voltage and outputs a sinusoidal current that is in phase with the utility voltage, yielding a power factor of unity.

***Index Terms*- Grid-connected, multilevel inverter, pulse-width modulated inverter (PWM), MATLAB/SIMULINK,**

I. INTRODUCTION

The solar power energy is turning out to be more essential since it creates less contamination and the expense of fossil fuel energy is rising, while the expense of solar arrays exhibits is decreased. Specifically, little limit appropriated power era system utilizing solar powered energy might be broadly utilized as a part of private applications earlier rather than later [1-2].

The power conversion interface is important to grid connected solar power generation systems because it converts the dc power generated by a solar cell array into ac power and feeds this ac power into the utility grid. An inverter is necessary in the power conversion interface to convert the dc power to ac power [2]–[4]. The power conversion efficiency of the power conversion interface is very important to guarantee there is no misuse of the energy produced by the solar cell array. In inverter there is a loss occurs due to active device and passive device. The power losses due to active devices include both conduction losses and switching losses [5].

Conduction loss results from the use of active devices, while the switching loss is proportional to the voltage and the current changes for each switching and switching frequency. The voltage change in every switching operation for a multi-level inverter is reduced in order to enhance its energy transformation efficiency [6]. The rival of switching harmonics is further attenuated, so the art loss caused all filter inductor is besides reduced. Therefore, MLI knowledge has been the summary of essentially research during the year days ago. The multilevel inverters should be designed by the whole of higher voltage levels in order to recover the conversion efficiency and to trim harmonic contents.

Multilevel inverter is normally having three types cascade H-bride, diode clamped and flying capacitor. The diode clamped [6-10] and flying capacitor [11-13] and cascade H-bridge inverters [14-18] are always used a capacitor to build up the several voltage steps. However, it is hard to control the voltage of these capacitors. Since it is hard to generate voltage knowledge in both the diode-clamped and the flying-capacitor topologies, the power circuit is difficult by the increase in the voltage levels that is essential for a multilevel inverter. For a seven level inverter used a 12 MOSFET switches in both diode clamped and flying capacitor network topologies also the cascade h-bridge MLI is to permit many stages of output voltage [17], so that cascade h-bridge inverter is always suitable for many application among improved voltage stages. So that in circuit topology two h-bridge inverter among dc bus voltage of multiple connection and is connected in cascade fashion to produce a single phase seven stage inverter and also used an 8 MOSFET switches. However in recent years, different types of topologies are proposed for seven stage inverter. For example, a single phase seven level grid connected inverter has been developed for solar power generation system [18]. So this type of seven level inverters normally connected in grid fashion which is having a 6 MOSFET switches. While three dc capacitors are using to construct a three voltage levels, which

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results in that balancing the voltages of capacitors is more difficult. So that proposed of seven levels inverter is configured as generation of level part and generation of polarity part [19]. As generation of level part is having only one power switches in high frequency, but using a ten MOSFET switches and three capacitors.

II. MULTI-LEVEL INVERTERS

As shown below figure 1 block diagram of multilevel inverter

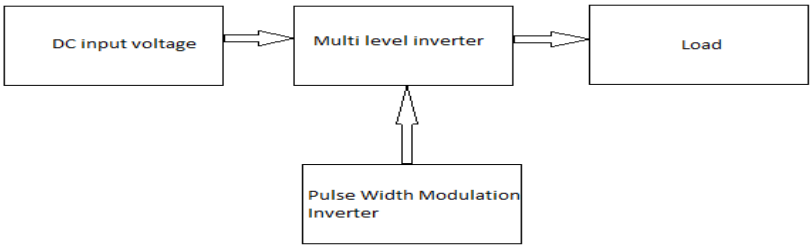

Fig 1: Multi-level Inverter

The **key features** of a multi-level structure are as follows:

The output voltage and power increase with number of levels. Adding a voltage level involves adding a main switching device to each phase. The harmonic content decreases as the number of levels increases and filtering requirements are reduced. With additional voltage levels, the voltage waveform has more free-switching angles, which can be reselected for harmonic elimination. In the absence of any PWM techniques, the switching losses can be avoided. Increasing output voltage and power does not require an increase in rating of individual device.

Static and dynamic voltage sharing among the switching devices is built into the structure through either clamping diodes or capacitors. The switching devices do not encounter any voltage-sharing problems. For this reason, multi-level inverters can easily be applied for high-power applications such as large motor drives and utility supplies. The fundamental output voltage of the inverter is set by the dc bus voltage Vdc, which can be controlled through a variable dc link. Multi-level approach includes good power quality, good electromagnetic compatibility (EMC), low switching losses, and high voltage capability.

III. CIRCUIT CONFIGURATION

Fig. 2 shows the configuration of the proposed solar power generation system. The proposed solar power generation system is composed of a solar cell array, a dc–dc power converter, and a new seven-level inverter. The solar cell array is connected to the dc–dc power converter, and the dc–dc power converter is a boost converter that incorporates a transformer with a turn ratio of 2:1.

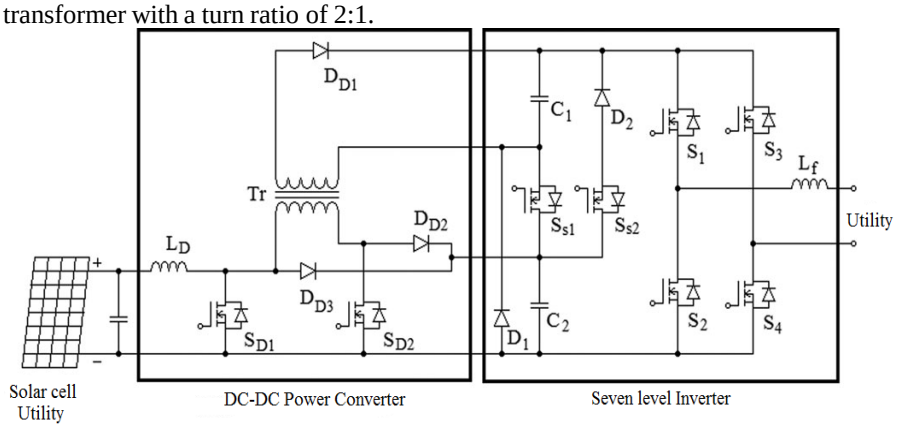

Fig 2: Configuration of the proposed solar power generation System

Fig. 2 shows the configuration of the proposed solar power generation system. The proposed solar power generation system is composed of a solar cell array, a dc–dc power converter, and a new seven-level inverter. The solar cell array is connected to the dc–dc power converter, and the dc–dc power converter is a boost converter that

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incorporates a transformer with a turn ratio of 2:1. The dc–dc power converter converts the output power of the solar cell array into two independent voltage sources with multiple relationships, which are supplied to the seven-level inverter. This new seven-level inverter is composed of a capacitor in a cascade. The power electronic switches of capacitor selection circuit and a full-bridge power converter, connected in a cascade. The power electronics switches of capacitor selection circuit determine the discharge of the two capacitors while the two capacitors are being discharged individually or in series. Because of the multiple relationships between the voltages of the dc capacitors, the capacitor selection circuit outputs a three-level dc voltage. The full-bridge power converter further converts this three-level dc voltage to a seven-level ac voltage that is synchronized with the utility voltage. In this way, the proposed solar power generation system generates a sinusoidal output current that is in phase with the utility voltage and is fed into the utility, which produces a unity power factor. As can be seen, this new seven-level inverter contains only six power electronic switches, so the power circuit is simplified.

IV. DC-DC POWER CONVERTER

As seen in Fig. 2, the DC–DC power converter incorporates a boost converter and a current-fed forward converter. The boost converter is composed of an inductor L_D, a power electronic switch S_{D1}, and a diode, D_{D3}. The boost converter charges capacitor C_2 of Seven level inverter. The current-fed forward converter is composed of an inductor L_D, power electronic switches S_{D1} and S_{D2}, a transformer, and diodes D_{D1} and D_{D2}. The current-fed forward converter charges capacitor C_1 of the seven-level inverter. The inductor L_D and the power electronic switch S_{D1} of the current-fed forward converter are also used in the boost converter.

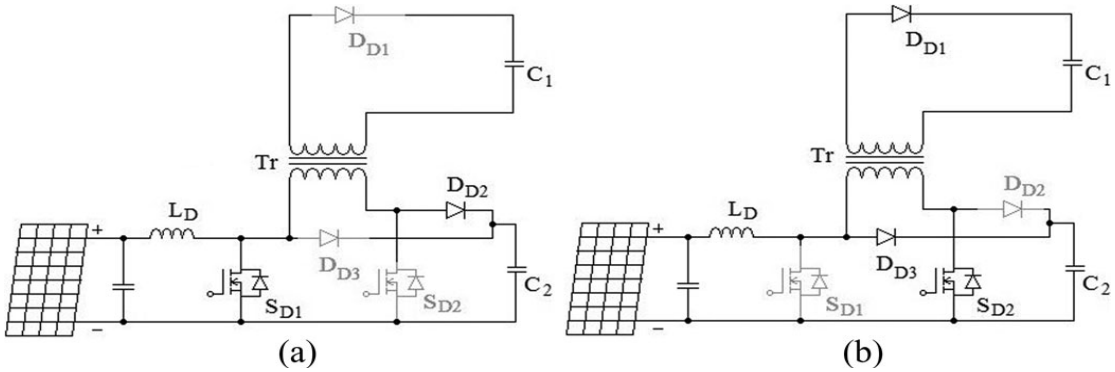

Fig 3: Operation of dc–dc power converter: (a) *SD*1 is on and (b) *SD*1 is off

Fig. 3(a) shows the operating circuit of the dc–dc power converter when S_{D1} is turned ON. The solar cell array supplies energy to the inductor L_D. When S_{D1} is turned OFF and $S_{D\,2}$ is turned ON, its operating circuit is shown in Fig. 3(b). Accordingly, capacitor C_1 is connected to capacitor C_2 in parallel through the transformer, so the energy of inductor L_D and the solar cell array charge capacitor C_2 through D_{D3} and charge capacitor C_1 through the transformer and D_{D1} during the off- state of $S_{D\,1}$. Since capacitors C1 and C2 are charged in parallel by using the transformer, the voltage ratio of capacitors C_1 and C_2 is the same as the turn ratio (2:1) of the transformer. There- fore, the voltages of C_1 and C_2 have multiple relationships. The boost converter is operated in the continuous conduction mode (CCM). The voltage of C_2 can be represented as

$$V_{c_2} = \frac{1}{1-D} V_s \qquad (1)$$

Where V_S is the output voltage of solar cell array and D is the duty ratio of $S_{D\,1}$. The voltage of capacitor C_1 can be represented as

$$V_{c_1} = \frac{1}{2(1-D)} V_s \qquad (2)$$

V. SEVEN LEVEL INVERTER

As seen in Fig. 2, the seven-level inverter is composed of a capacitor selection circuit and a full-bridge power converter, which are connected in cascade. The operation of the seven- level inverter can be divided into the positive half cycle and the negative half cycle of the utility. For ease of analysis, the **power electronic switches** and diodes are assumed to be ideal, while the voltages of both capacitors C_1 and C_2 in the capacitor selection circuit are

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constant and equal to $V_{dc}/3$ and $2V_{dc}/3$, respectively. Since the output current of the solar power generation system will be controlled to be sinusoidal and in phase with the utility voltage, the output current of the seven-level inverter is also positive in the positive half cycle of the utility. The operation of the seven-level inverter in the positive half cycle of the utility can be further divided into four modes, as shown in Fig. 4.

Mode 1: The operation of mode 1 is shown in Fig. 4(a). Both S_{S1} and S_{S2} of the capacitor selection circuit are OFF, so C_1 is discharged through D_1 and the output voltage of the capacitor selection circuit is $V_{dc}/3$. S_1 and S_4 of the full-bridge power converter are ON. At this point, the output voltage of the seven-level inverter is directly equal to the output voltage of the capacitor selection circuit, which means the output voltage of the seven-level inverter is $V_{dc}/3$.

Mode 2: The operation of mode 2 is shown in Fig. 4(b). In the capacitor selection circuit, S_{S1} is OFF and S_{S2} is ON, so C_2 is discharged through S_{S2} and D_2 and the output voltage of the capacitor selection circuit is $2V_{dc}/3$. S_1 and S_4 of the full-bridge power converter are ON. At this point, the output voltage of the seven-level inverter is $2V_{dc}/3$.

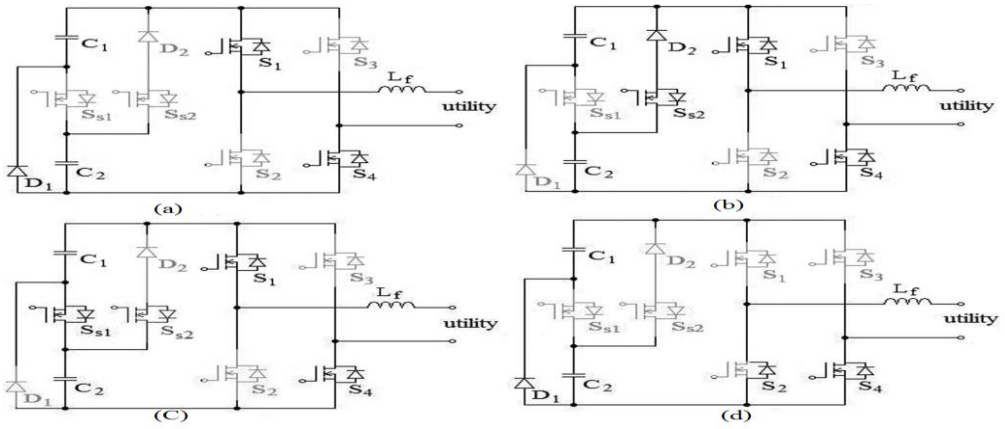

Fig 4: Operation of the seven-level inverter in the positive half cycle, (a) mode 1, (b) mode 2, (c) mode 3, and (d) mode 4

Mode 3: The operation of mode 3 is shown in Fig. 4(c). In the capacitor selection circuit, S_{S1} is ON. Since D_2 has a reverse bias when S_{S1} is ON, the state of S_{S2} cannot affect the current flow. Therefore, S_{S2} may be ON or OFF, to avoiding switching of S_{S2}. Both C_1 and C_2 are discharged in series and the output voltage of the capacitor selection circuit is V_{dc}. S_1 and S_4 of the full-bridge power converter are ON. At this point, the output voltage of the seven-level inverter is V_{dc}.

Mode 4: The operation of mode 4 is shown in Figure.4 (d). Both S_{S1} and S_{S2} of the capacitor selection circuit are OFF. The output voltage of the capacitor selection circuit is $V_{dc}/3$. Only S_4 of the full-bridge power converter is ON. Since the output current of the seven-level inverter is positive and passes through the filter inductor, it forces the anti-parallel diode of S_2 to be switched ON for continuous conduction of the filter inductor current. At this point, the output voltage of the sevens level inverter is zero.

In the negative half cycle, the output current of the seven level inverter is negative. The operation Seven level inverter can also be further divided into four modes, as shown in Fig. 5. A comparison with Fig. 4 shows that the operation of the capacitor selection circuit in the negative half cycle is the same as that in the positive half cycle. The difference is that S_2 and S_3 of the full-bridge power converter are ON during modes 5, 6, and 7, and S_2 is also ON during mode 8 of the negative half cycle. Accordingly, the output voltage of the capacitor selection circuit is inverted by the full-bridge power converter, so the output voltage of the seven-level inverter also has four levels: $-V_{dc}$, $-2V_{dc}/3$, $-V_{dc}/3$, and 0.

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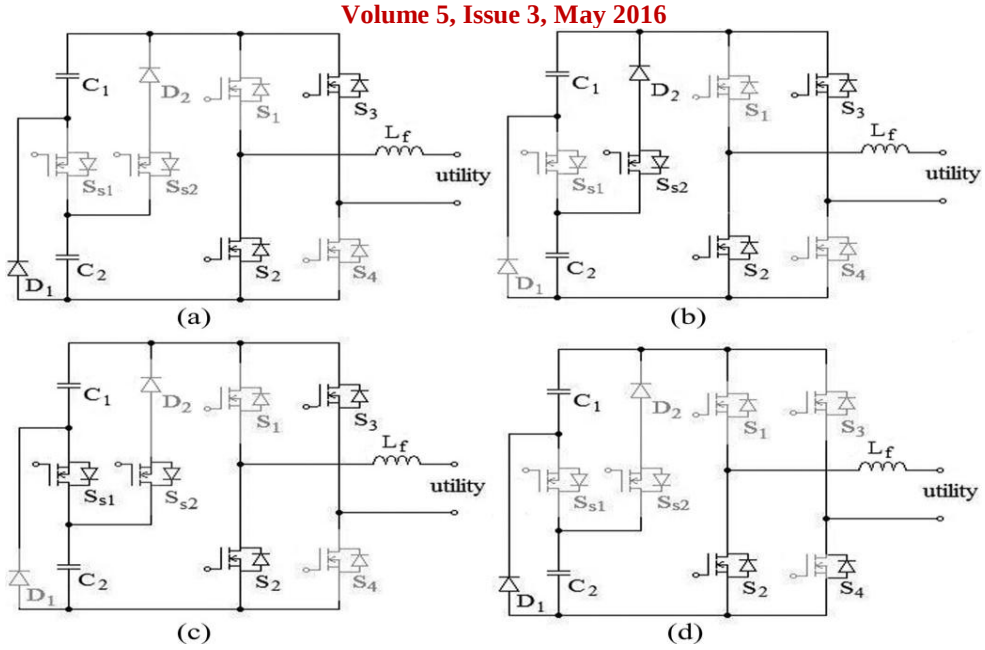

Fig 5: operation of the seven level inverter in the negative half cycle (a) mode 5, (b) mode 6, (c) mode 7, (d) mode 8.

VI. SIMULATION OF MULTILEVEL INVERTER

1. Simulation result of single phase single level inverter(full bridge inverter)

As shown above Figure 6 of single phase single level inverter. When S_1 and S_2 are switched on, the input voltage +Vs appears across the load. If S_3 and S_4 are switched on, the vtg across the load is reversed -Vs.
The RMS output voltage of Single level inverter is

$$V_0 = V_s$$

The RMS value of fundamental Components is

$$V_{01} = \frac{4Vs}{\pi\sqrt{2}} = 0.90Vs$$

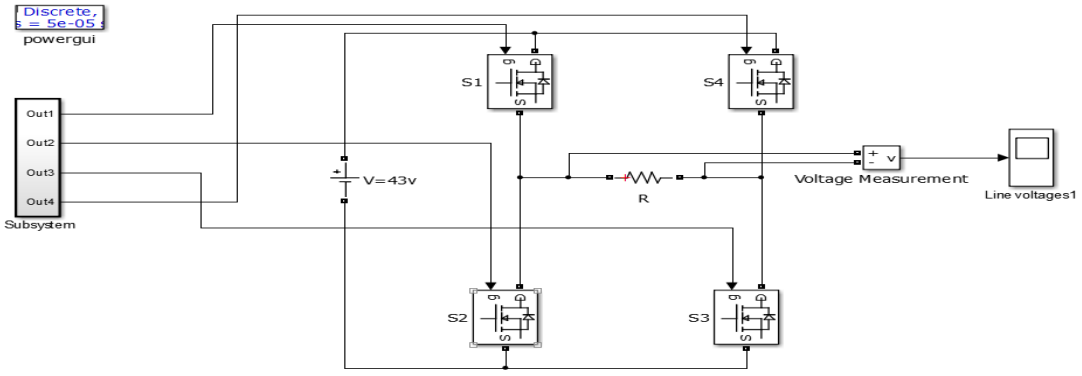

Fig 6: Simulation of Single phase full bridge inverter

In the below figure 7 shows that single phase single level inverter waveform where x-axis is Time and y-axis is Voltage

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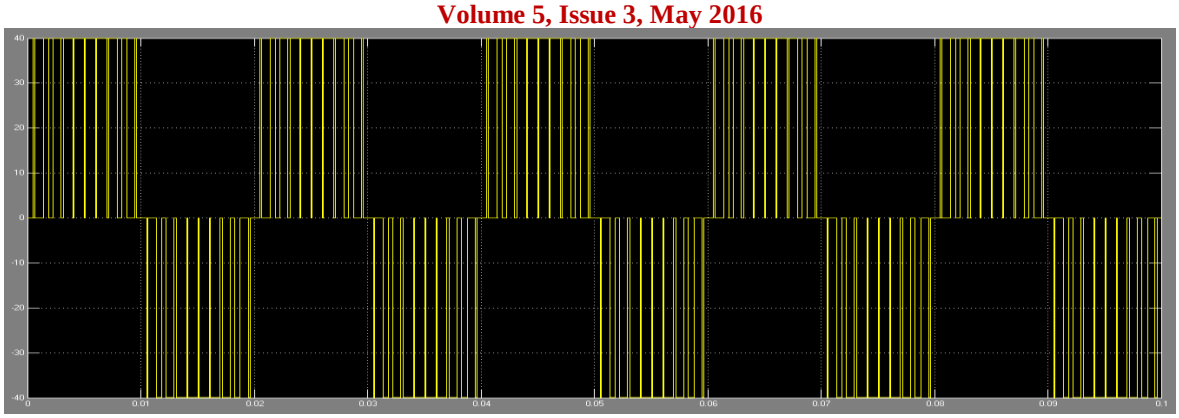

Fig 7: Single phase full bridge inverter output waveform (Voltage V/S Time)

In the below figure 8 shows that FFT analysis of Single Phase full bridge inverter or Single Phase Single level inverter where total harmonic distortion (THD) is 54.03%.

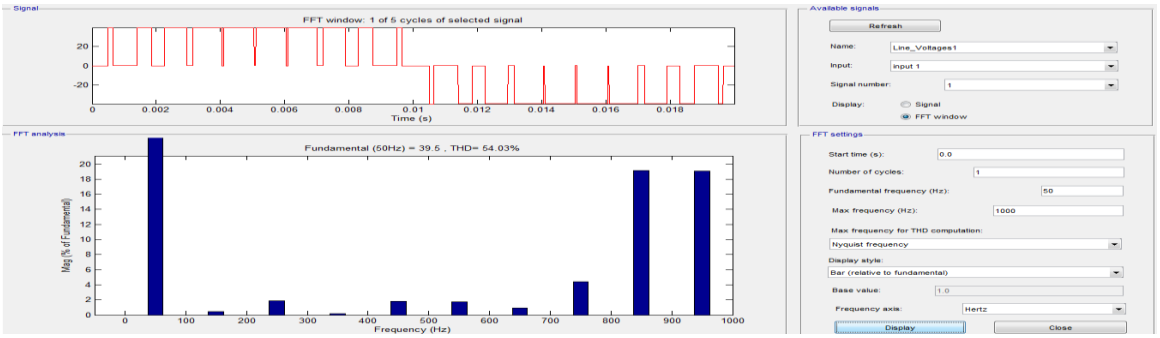

Fig 8: Single phase full bridge inverter FFT analysis

2. Simulation results of single phase Three level diode clamped inverter

A single phase three level diode clamped inverter as shown in below Fig 9 When L_{1a}, L_{1b} & L_{2c}, L_{2d} are turned on simultaneously. Similarly the L_{1c}, L_{1d} & L_{2a}, L_{2b} are turned on simultaneously such that the rms of output voltage across to the load is

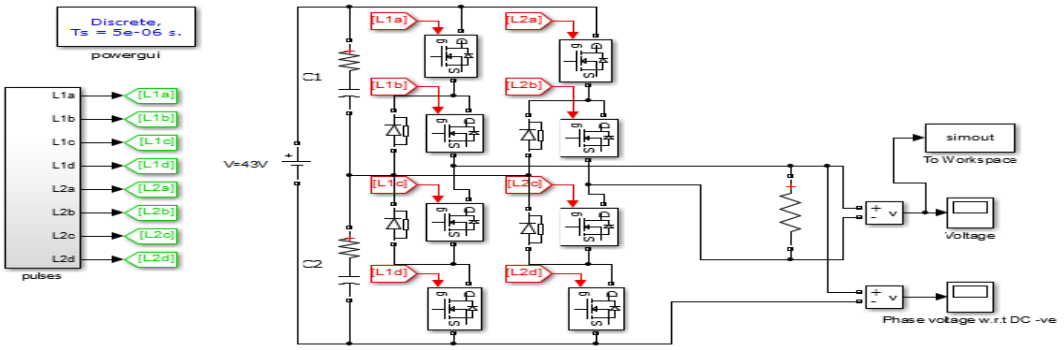

Fig 9: Simulation of Single Phase Three level diode clamped inverter

The RMS output voltage of Single phase three level inverter is

$$V_0 = \frac{2}{\sqrt{3}} V_s$$

The RMS value of fundamental Components is

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$$V_{01} = \frac{6V_s}{\pi\sqrt{2}}$$

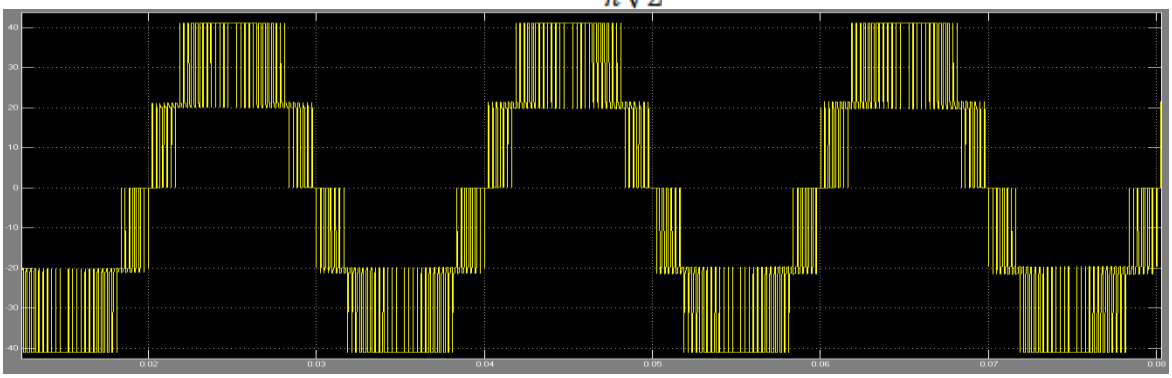

Fig 10: Single phase three level diode clamped inverter output waveform (Voltage V/S Time)

In the below figure 11 shows that FFT analysis of Single phase three level diode clamped inverter where total harmonic distortion (THD) is 27.05%.

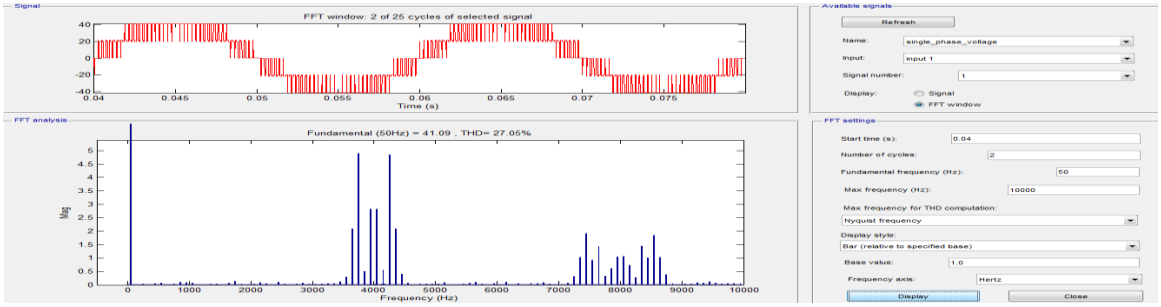

Fig11: Single phase three level Diode Clamped inverter FFT analysis

3. Simulation results of Single phase Seven level inverter

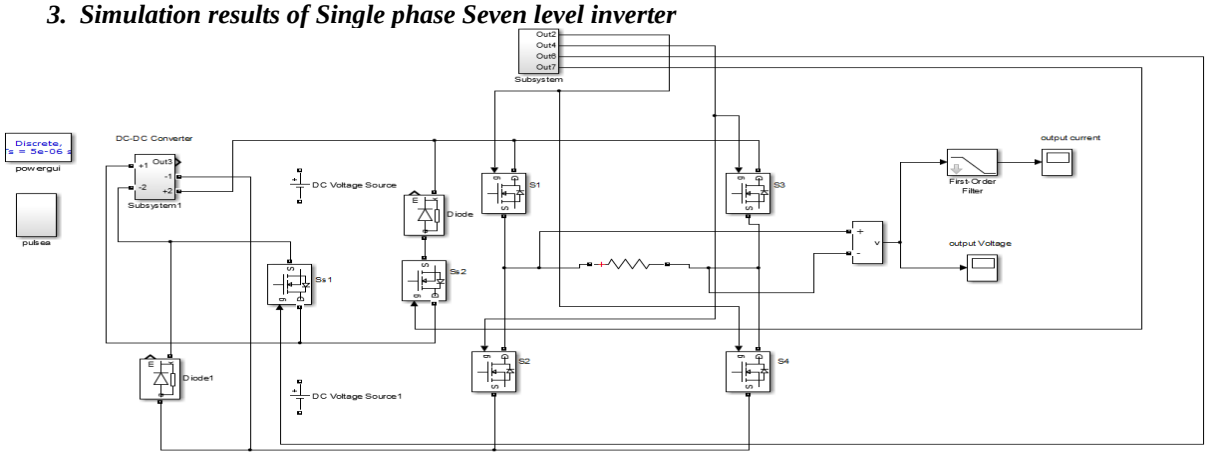

Fig 12: Simulation of Single Phase Seven Level inverter

In the below Table1 shows that states of switches and device operating in positive and negative mode of seven level inverter

Table 1: States of switches and devices operating in Positive and Negative mode

V_o	S_1	S_2	S_3	S_4	S_{S1}	S_{S2}	$C_1(V_{dc}/3)$	$C_2(2V_{dc}/3)$
$V_{dc}/3$	1	0	0	1	0	0	$V_{dc}/3$	-
$2V_{dc}/3$	1	0	0	1	0	1	-	$2V_{dc}/3$

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V_{dc}	1	0	0	1	1	0	$V_{dc}/3$	$2V_{dc}/3$
0	0	0(D_2On)	0	1	0	0	-	-
$-V_{dc}/3$	0	1	1	0	0	0	$-V_{dc}/3$	-
$-2V_{dc}/3$	0	1	1	0	0	1	-	$-2V_{dc}/3$
$-V_{dc}$	0	1	1	0	1	0	$-V_{dc}/3$	$-2V_{dc}/3$
0	0	1	0	0(D_4On)	0	0	-	-

In the below fig 13 shows seven level inverter output voltage waveform where x-axis is Time and y-axis is Voltage

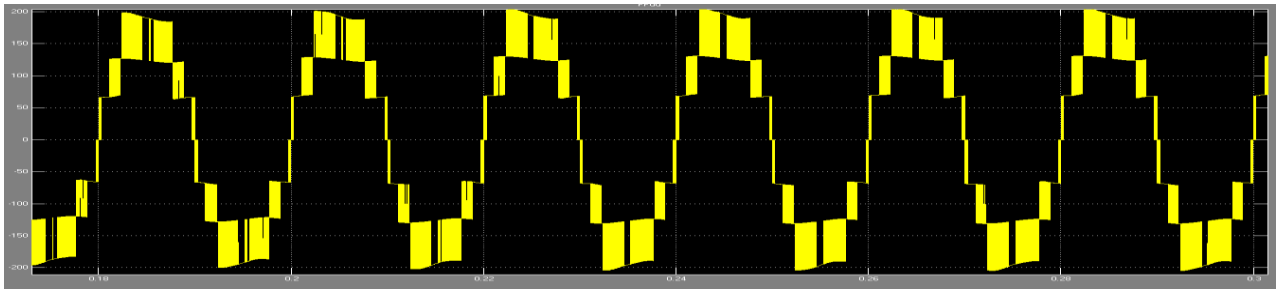

Fig 13: Single Phase Seven Level inverter output Voltage waveform (Voltage v/s Time)

Fig 14: Single Phase Seven Level inverter output Current waveform (Current v/s Time)

In the above figure 14 shows seven level inverter output current waveform where x-axis is Time and y-axis is Current

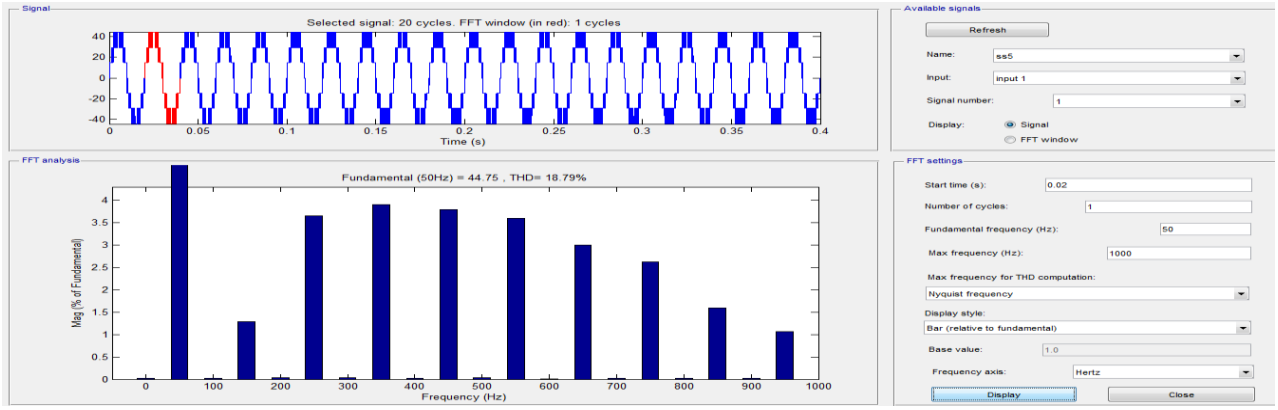

Fig15: Single phase Seven level inverter FFT analysis

In the above figure 15 shows that FFT analysis of Single phase Seven level inverter where total harmonic distortion (THD) is 18.79%

4. Comparisons of Multilevel Inverters

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From the below table 2 shows that comparison of multilevel inverters. As increasing the level of inverters such that total harmonic distortion become reduces.

Table 2: Comparison of Multilevel Inverters

Phase	Multilevel inverter	Level	DC Voltage	Total Harmonic Distortion
Single	Full bridge	Single Level	43V	54.062%
Single	Diode clamped	Three Level	43V	27.03%
Single	Cascaded H-bridge	Seven Level	43V	18.79%

VII. CONCLUSION

This paper proposes a solar power generation system to convert the dc energy generated by a solar cell array into ac energy that is fed into the utility. The proposed solar power generation system is composed of a dc–dc power converter and a seven- level inverter. The seven-level inverter contains only six power electronic switches, which simplifies the circuit configuration. Furthermore, only one power electronic switch is switched at high frequency at any time to generate the seven-level output voltage. This reduces the switching power loss and improves the power efficiency. The voltages of the two dc capacitors in the proposed seven-level inverter are balanced automatically, so the control circuit is simplified. Simulation results show that the proposed solar power generation system generates a seven-level output voltage and outputs a sinusoidal current that is in phase with the utility voltage, yielding a power factor of unity and also as increasing the level of inverters such that total harmonic distortion (THD) is reduces.

REFERENCES

[1] R. A. Mastromauro, M. Liserre, and A. Dell'Aquila, "Control issues in single-stage photovoltaic systems: MPPT, current and voltage control," IEEE Trans. Ind. Informat., vol. 8, no. 2, pp. 241–254, May. 2012.

[2] Z. Zhao, M. Xu,Q. Chen, J. S. Jason Lai, andY. H. Cho, "Derivation, analysis, and implementation of a boost–buck converter-based high-efficiency PV inverter," IEEE Trans. Power Electron., vol. 27, no. 3, pp. 1304–1313, Mar. 2012.

[3] M. Hanif, M. Basu, and K. Gaughan, "Understanding the operation of a Z-source inverter for photovoltaic application with a design example," IET Power Electron., vol. 4, no. 3, pp. 278–287, 2011.

[4] J.-M. Shen, H. L. Jou, and J. C. Wu, "Novel transformer-less grid connected power converter with negative grounding for photovoltaic generation system," IEEE Trans. Power Electron., vol. 27, no. 4, pp. 1818–1829, Apr. 2012.

[5] N. Mohan, T. M. Undeland, and W. P. Robbins, Power Electronics Converters, Applications and Design, Media Enhanced 3rd ed. New York, NY, USA: Wiley, 2003.

[6] K. Hasegawa and H. Akagi, "Low-modulation-index operation of a five level diode-clamped pwm inverter with a dc-voltage-balancing circuit for a motor drive," IEEE Trans. Power Electron., vol. 27, no. 8, pp. 3495–3505, Aug. 2012.

[7] E. Pouresmaeil, D. Montesinos-Miracle, and O. Gomis-Bellmunt, "Control scheme of three-level NPC inverter for integration of renewable energy resources into AC grid," IEEE Syst. J., vol. 6, no. 2, pp. 242–253, Jun.2012.

[8] S. Srikanthan and M. K. Mishra, "DC capacitor voltage equalization in neutral clamped inverters for DSTATCOM application," IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2768–2775, Aug. 2010.

[9] M. Chaves, E. Margato, J. F. Silva, and S. F. Pinto, "New approach in back-to-back m-level diode clamped multilevel converter modeling and direct current bus voltages balancing," IET power Electron., vol. 3, no. 4, pp. 578–589, 2010.

[10] J. D. Barros, J. F. A. Silva, and E. G. A Jesus, "Fast-predictive optimal control of NPC multilevel converters," IEEE Trans. Ind. Electron., vol. 60, no. 2, pp. 619–627, Feb. 2013.

[11] A. K. Sadigh, S. H. Hosseini, M. Sabahi, and G. B. Gharehpetian, "Double flying capacitor multicell converter based on modified phase-shifted pulse width modulation," IEEE Trans. Power Electron., vol. 25, no. 6, pp. 1517–1526, Jun. 2010.

[12] S. Thielemans, A. Ruderman, B. Reznikov, and J. Melkebeek, "Improved natural balancing with modified phase-shifted PWM for single-leg five level flying-capacitor converters," IEEE Trans. Power Electron., vol. 27,no. 4, pp. 1658–1667, Apr. 2012.

[13] S. Choi and M. Saeedifard, "Capacitor voltage balancing of flying capacitor multilevel converters by space vector PWM," IEEE Trans. Power Delivery, vol. 27, no. 3, pp. 1154–1161, Jul. 2012.

ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 5, Issue 3, May 2016

[14] L. Maharjan, T. Yamagishi, and H. Akagi, "Active-power control of individual converter cells for a battery energy storage system based on a multilevel cascade pwm converter," IEEE Trans. Power Electron., vol. 27, no. 3, pp. 1099–1107, Mar. 2012.

[15] X. She, A. Q. Huang, T. Zhao, and G. Wang, "Coupling effect reduction of a voltage-balancing controller in single-phase cascaded multilevel converters," IEEE Trans. Power Electron., vol. 27, no. 8, pp. 3530–3543, Aug. 2012.

[16] J. Chavarria, D. Biel, F. Guinjoan, C. Meza, and J. J. Negroni, "Energy balance control of PV cascaded multilevel grid-connected inverters under level-shifted and phase-shifted PWMs," IEEE Trans. Ind. Electron, vol. 60, no. 1, pp. 98–111, Jan. 2013.

[17] J. Pereda and J. Dixon, "High-frequency link: A solution for using only one DC source in asymmetric cascaded multilevel inverters," IEEE Trans. Ind. Electron., vol. 58, no. 9, pp. 3884–3892, Sep. 2011.3462 IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 29, NO. 7, JULY 2014.

[18] N. A. Rahim, K. Chaniago, and J. Selvaraj, "Single-phase seven-level grid-connected inverter for photovoltaic system," IEEE Trans. Ind. Electr. vol. 58, no. 6, pp. 2435–2443, Jun. 2011.

[19] Y. Ounejjar, K. Al-Hadded, and L. A. Dessaint, "A novel six-band hysteresis control for the packed U cells seven-level converter: Experimental validation," IEEE Trans. Ind. Electron., vol. 59, no. 10, pp. 3808–3816, Oct. 2012.

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