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GDI Based Design of Low Power Adders and Multipliers

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Abstract: ***The multiplication and addition are the important operations in RISC Processor and DSP units. Specifically, speed and power efficient implementations of adders and multipliers are very challenging. With the increase in complexity of VLSI systems and minimizing power consumption has clearly become a priority. The architecture of Adders like Ripple Carry Adder, Carry Look Ahead Adder, Kogge-Stone Adder and Brent-Kung Adders have advantages with respect to power, area and complexity. The architecture of Multipliers like Braun and Wallace Tree Multipliers are efficient and easy to design when compared to other multipliers. Further to reduce power consumption, instead of adders, 3:2, 4:3, 5:3, 6:3 and 7:3 compressors are used for the addition of partial products in multipliers. Further to reduce power consumption in the adders, compressors and multipliers using a new technique called Gate Diffusion Input (GDI) instead of Complementary Metal Oxide Semiconductor (CMOS). So, these GDI based design of multipliers using compressors and these GDI based design of these Adders may reduce power consumption compared to that of design in CMOS. Tanner Tool is using to design the above.***

Index terms: **Gate Diffusion Input (GDI), Complementary Metal Oxide Semiconductor (CMOS), Digital Signal Processing (DSP).**

I. INTRODUCTION

With the advances in Very Large Scale Integration (VLSI) technology, arithmetic operations are penetrating into more and more applications. The basic operation found in most arithmetic components is the binary addition and Multiplication. Computations needs to be performed using low-power, area-efficient circuits operating at greater speed. Addition is the most basic arithmetic operation; and adder is the most fundamental arithmetic component of the processor. In addition, each of the resulting output bits are depending on its corresponding inputs. It is very important operation because it involves a carry ripple step i.e the carry from the previous bits addition should propagates to next bits of addition.

Multiplication is an operation that occurs frequently in digital signal processing and many other applications.[1] Multipliers occupy more area so that it consumes large delay when compared to Adders. Therefore several techniques are being proposed to speed up the computation while maintaining the less or reasonable area. A multiplier can be divided into three stages: The first stage is Partial products generation stage, second is partial products addition stage, and the final is addition stage. In the first stage, the multiplier and the multiplicand are multiplied bit by bit to generate the partial products. The second stage is more complicated and it determines the speed of the overall multiplier. In this stage the partial products generated by the previous stage is added by using Adders or compressors depending on the technique used for designing multipliers.

The present development in processor designs aim is design of low power multiplier. So, the need for low power multipliers has increased. Generally the computational performance of DSP processors is affected by its multipliers performance. This results in circuit delay because to perform the addition of next bits, it should wait until the completion of addition from the previous bits. So that it propagates carry to the next stage Designers of VLSI have several options to reduce the power dissipation in the various design stages. Recently, the requirement of portability and the moderate improvement in battery performance indicate that the power dissipation is one of the most critical design parameters. The three most widely accepted metrics to measure the quality of a circuit or to compare various circuit styles are area, delay and power still demands high computational speeds. The architecture of Adders like Ripple Carry Adder, Carry Look Ahead Adder, Kogge-Stone Adder and Brent-Kung Adders have advantages with respect to power, area and complexity. The architecture of Multipliers like Braun and Wallace Tree Multipliers are efficient and easy to design when compared to other multipliers. Further to reduce power consumption, instead of adders, 3:2, 4:3, 5:3, 6:3 and 7:3 compressors are used for the addition of partial products in multipliers. Further to reduce power consumption in the adders, compressors and multipliers, a new technique called Gate Diffusion Input (GDI) is used instead of Complementary Metal Oxide Semiconductor (CMOS).

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II. GATE DIFFUSION INPUT (GDI) STRUCTURE

Gate diffusion input (GDI) — A new technique of low-power digital combinational circuit design. This technique allows reducing power consumption, propagation delay, and area of digital circuits while maintaining low complexity of logic design. Pass-transistor logic has been presented for NMOS. They are based on the model, where a set of control signals is applied to the gates of NMOS transistors. Another set of data signals are applied to the sources of the n-transistors. Some of the main advantages of PTL over standard GDI design are

High speed, due to the small node capacitances

- Low power dissipation, as a result of the reduced number of transistors
- Lower interconnection due to a small area.
- However, most of the PTL implementations have two basic problems. They are:
- Since the "high input voltage level at the regenerative inverters is not VDD, the PMOS device in the inverter is not fully turned off, and hence Direct-path static power dissipation could be significant

A new low-power design technique that allows solving most of the problems mentioned above - GDI technique. The GDI approach allows implementation of a wide range of complex logic functions using only two transistors. This method is suitable for design of fast, low-power circuits, using a reduced number of transistors (as compared to GDI and existing PTL techniques), while improving logic level swing and static power characteristics and allowing simple top-down design by using small cell library.

The GDI method is based on the use of a simple cell as shown in Figure..1 At first glance, the basic cell reminds one of the standard GDI inverter, but there are some important differences.[1]

- The GDI cell contains three inputs G(common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of NMOS).
- Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased in contrast with a GDI inverter.

It must be remarked that not all of the functions are possible in standard p-well GDI process but can be successfully implemented in twin-well GDI or silicon on insulator (SOI) technologies. Table 1 shows how a simple change of the input configuration of the simple GDI cell corresponds to very different Boolean functions. Most of these functions are complex (6-12 transistors) in GDI, as well as in standard PTL implementations, but very simple (only two transistors per function) in the GDI design method

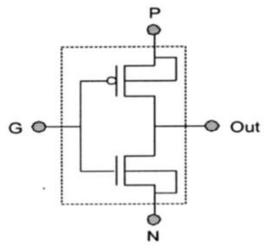

Fig.1: GDI Basic Cell [[1]

Table.1: Various Logic Functions of GDI cell for different Input configurations[1]

N	P	G	OUT	FUNCTION
0	B	A	A'B	F1
B	1	A	A'+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B+AC	MUX
0	1	A	A'	NOT

III. CMOS VS GDI STRUCTURE

Complementary metal–oxide–semiconductor (CMOS) is a technology for constructing integrated circuits. CMOS technology is used in microcontroller, microprocessor, static RAM and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors (CMOS sensors), data converters, and highly integrated transceivers for many types of communication. Two CMOS is also sometimes

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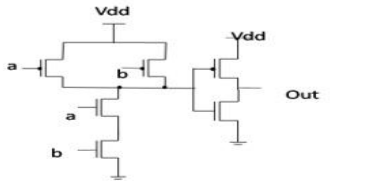
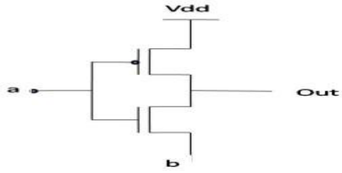
referred to as complementary-symmetry metal–oxide–semiconductor (or COS-MOS).[1] The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide field effect transistors (MOSFETs) for logic functions. Important characteristics of CMOS devices are high noise immunity and low static power consumption. CMOS circuits are constructed in such a way that all PMOS transistors should have either an input from the voltage source or from another PMOS transistor. Similarly, all NMOS transistors should have either an input from ground or from another NMOS transistor. The composition of a PMOS transistor provides low resistance between its source and drain contacts when a low gate voltage is applied and high resistance when a high gate voltage is applied. But on the other hand, the composition of an NMOS transistor provides high resistance between source and drain when a low gate voltage is applied and low resistance when a high gate voltage is applied. CMOS achieves current reduction by complementing every NMOSFET with a PMOSFET and connecting both gates and both drains together. [2] A high voltage on the gates will result to the condition that NMOSFET will conduct and the PMOSFET will not conduct while a low voltage on the gates causes the reverse. This technique greatly reduces power consumption and heat production. However, during the switching time both MOSFETs conduct briefly as the gate voltage goes from one state to another. GDI resembles standard CMOS inverter cell with the only difference is that CMOS inverter has only one input and two supply voltages VDD and VSS. But GDI cell can have three inputs G (common gate input of NMOS and PMOS), VDD supply is replaced by P (input to the source/drain of PMOS), VSS supply is replaced by N (input to the source/drain of NMOS).

IV. IMPLEMENTATION

Table 2 implementation of logic gates using GDI technique and CMOS [2]

<table>
<tr><th></th><th>CMOS</th><th>GDI</th></tr>
<tr><td>AND</td><td>
</td><td>
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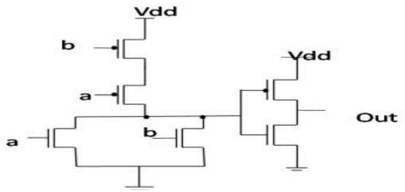
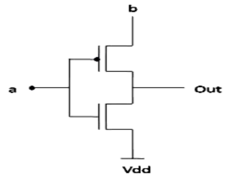
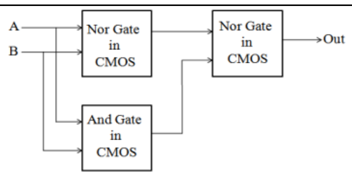
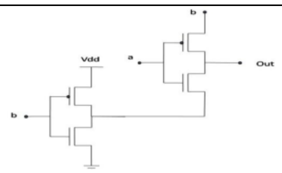
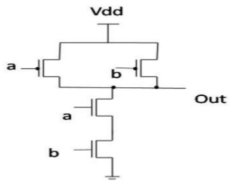
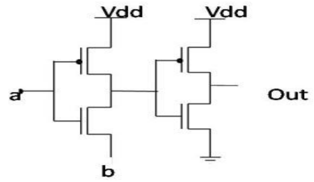
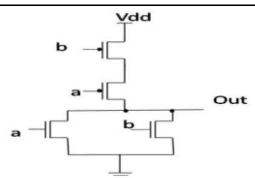
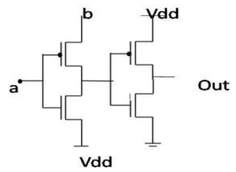
<tr><td>OR</td><td>
</td><td>
</td></tr>
<tr><td>XOR</td><td>
</td><td></td></tr>
<tr><td>NAND</td><td>
</td><td>
</td></tr>
<tr><td>NOR</td><td>
</td><td>
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</table>

A. Ripple Carry Adder

This is also known as parallel adder. In this all the bits are given simultaneously. For a 4-bit adder its consists of 4 stages and each stage consists of one full adder. At each stage carry is calculated starting from lower bit. This carry is propagated to the next stage. The main advantage of this RCA is simplicity. The main disadvantages of this RCA are that the carry should be propagated through each stage to get the final output which takes large amount of time. [4]The below figure represents the Logic diagram of the 4-bit Ripple Carry Adder with a two input busses each of 4-bit length namely A<3:0> , B<3:0> and C_{in} as Carry input and sum<3:0> as output bus of 4-bit length and C_{out} as carry out.

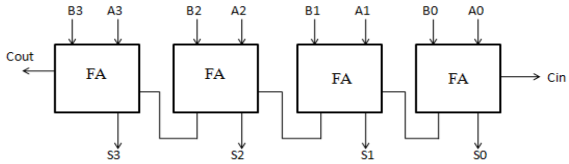

Fig 2: Logic diagram of 4-bit Ripple Carry Adder

By cascading two 4-bit RCA we will obtain a 8-bit RCA Logic diagram of the 8-bit Ripple Carry Adder with a two input busses each of 8-bit length namely A<7:0>, B<7:0> and C_{in} as Carry input and sum<7:0> as output bus of 8-bit length and C_{out} as carry out is shown in the below figure 3

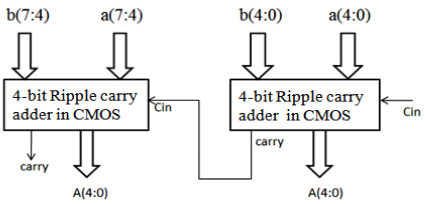

Fig 3: Logic diagram of 8-bit RCA

B. Carry Look Ahead Adder (CLA)

It is faster especially in adding large number of bits. A carry-look ahead adder improves speed by reducing the amount of time required to determine carry bits. By using a carry look ahead carry generator can easily construct a 4-bit parallel adder. Each sum requires two exclusive-OR gates. The output of first exclusive-OR generates Pi, and the AND gate generates Gi. The carriers are generated using look ahead carry generator and applied as inputs to the second exclusive-OR gate. Other input to exclusive-OR gates is Pi. Thus second exclusive-OR gate generates sum outputs. Each output each generated after a delay of two levels gates. Thus, outputs S0 through S3 have equal propagation delay times. It can be contrasted with the simpler, but usually slower, ripple carry adder for which the carry bit is calculated alongside the sum bit, and each bit must wait until the previous carry has been calculated to begin calculating its own result and carry bits The carry-look ahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bit. Carry look ahead adder is able to generate carries before the sum is produced using propagate and generate logics to make addition much faster. From the full adder circuit derived two functions carry generator and carry propagate logic.

$$\text{Generate, } Gi = Ai \text{ AND } Bi$$
$$\text{Propagate, } Pi = (Ai \text{ XOR } Bi)$$

The output sum and carry can be expressed as

$$\text{Sum, } Si = Pi \text{ xor } Ci$$
$$\text{Carry, } Ci+1 = Gi + PiCi$$

Gi is called a carry generate and it produces on carry when both Ai and Bi are one, regardless of the input carry. Pi is called a carry propagate because it is term associated with the propagation of the carry from Ci to Ci+1. Now the Boolean functions for the carry output of each stage can be written as follows,

$$C2=G1+P1C1$$
$$C3 = G2+P2C2 = G2+P2\,(G1+P1C1) = G2+P2G1+P2P1C1$$
$$C4=G3+P3C3$$

From the above equations C4 does not have to wait for C3 and C2 to propagate, in fact C4 is propagated at the same time as C2 and C3. The Boolean functions for each output carry are expressed in sum of product form, thus

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they can be implemented using AND-OR logic. By combining multiple carry look ahead adders even larger adders can be implemented. This can be used at multiple levels to make even larger adders

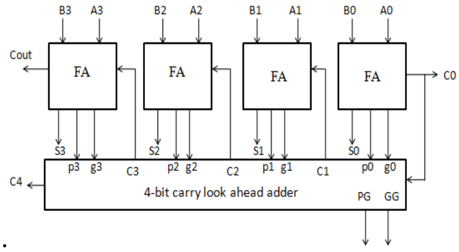

Fig 4: Logic diagram of 4-Bit Carry Look Ahead Adder

Logic diagram of the 8-bit Carry Look Ahead Adder with a two input busses each of 8-bit length namely A<7:0> , B<7:0> and C_{in} as Carry input and sum<7:0> as output bus of 8-bit length and C_{out} as carry out is shown in the figure 5

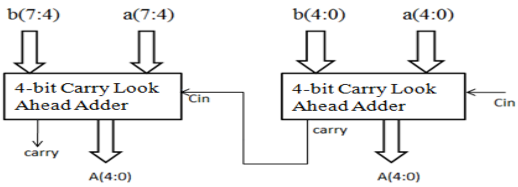

Fig 5: Logic diagram of 8-Bit CLA Adder

V. IMPLEMENTATION OF 8-BIT PARALLEL PREFIX ADDERS

It is the fastest adder used in industries. The parallel prefix addition is done in 3 steps. They are:

1. Pre-processing stage
2. Carry generation network
3. Post processing stage

In this Pre-processing stage we compute, the generate and propagate signals are used to generate carry input of each adder. A and B are inputs. These signals are given by the equation 1&2. [7]

$$P_i = A_i \text{ Xor } B_i \qquad (1)$$

$$G_i = A_i \text{ And } B_i \qquad (2)$$

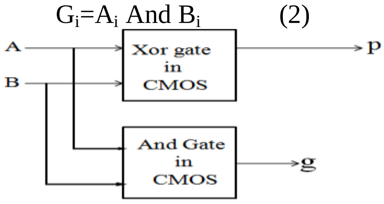

Fig 6: Pre-processing stage

In this Carry generation network stage we compute carries corresponding to each bit. Execution is done in parallel form. After the computation these. carry operator contain two AND gates, one OR gate. It uses propagate and generate as intermediate signals which are given by the equations 3&4.

$$P_{(i:k)} = P_{(i:j)} \cdot P_{(j-1:k)} \qquad (3)$$

$$G_{(i:k)} = G_{(i:i)} + (G_{(i-1:k)} \cdot P_{(i:j)}) \qquad (4)$$

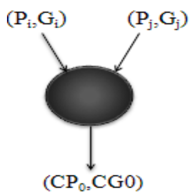

Fig 7: Carry operator. [7]

The operations involved in this figure are given as.

$$CP_0 = P_i \text{ and } P_j \qquad (3(i))$$

$$CG_0 = (P_i \text{ and } G_j) \text{ or } G_i \qquad (3(ii))$$

Where P_i,G_i are present bits and P_j,G_j are the previous bits

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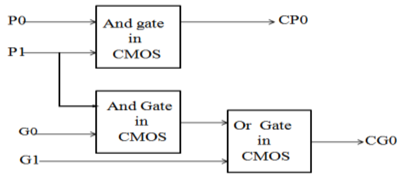

Fig 8: Carry generation network of Kogge-Stone Adder

This Post processing stage is the final stage to compute the summation of input bits. it is same for all adders and sum bit equation given

$$S_i = P_i \text{ Xor } C_i \qquad (5)$$

$$C_{i+1} = (P_i . C_0) + G_i \qquad (6)$$

Kogge-Stone Adder and Brent-Kung Adders design in CMOS logic of 8-bit are discussed below. The logic diagrams and the corresponding inner block logic diagrams are clearly represented below.

A. Kogge-Stone Adder

Kogge-Stone prefix adder is a fast adder design. Kogge-Stone adder has best performance in VLSI implementations. It has large area with minimum fan-out and it is also known as a parallel prefix adder that performs fast logical addition. [6]Kogge-Stone adder is used for wide adders because of it shows the less delay among other architectures. Each vertical stage produce Propagate and Generate bits. Generate bits are produced in the last stage and these bits are XORed with the initial propagate after the input to produce the sum bits. Logic diagram of the 8-bit Kogge-Stone Adder with a two input busses each of 8-bit length namely A<7:0> , B<7:0> and C_{in} as Carry input and sum<7:0> as output bus of 8-bit length and C_{out} as carry out are shown in the figure 4.7.

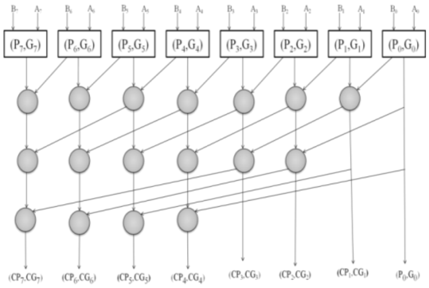

Fig 9: Logic diagram of 8-Bit Kogge-Stone Adder[6]

B. Brent-Kung Adder

The Brent-Kung adder is a parallel prefix adder. Brent-Kung has maximum logic depth and minimum area. The number of cells is calculated by using 2(n-1) -Log_2n .[5].Logic Diagram of the 8-bit Brent-Kung Adder with a two input busses each of 8-bit length namely A<7:0> , B<7:0> and C_{in} as Carry input and sum<7:0> as output bus of 8-bit length and C_{out} as carry out is shown in the figure 10.

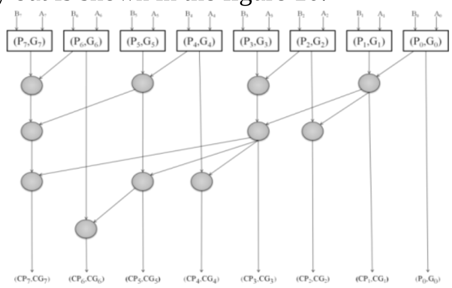

Fig 10: Logic diagram of 8-Bit Brent-Kung Adder [5]

VI. BRAUN MULTIPLIER

An nxn-bit Braun Multiplier requires n(n-1) adders and n^2AND gates. This makes Braun multipliers ideal in VLSI and ASIC realization. Each of the X_iY_j product bits is generated in parallel with the AND gates. Each partial product can be added to the previous sum of partial products by using a row of adders. The vary-out signals are shifted one bit to the left and are then added to the sums of the first adder and the new partial product. As the carry bits are passed diagonally downward to the next adder stage, there is no horizontal carry propagation for the subsequent adder stage. The Schematic of 8x8 Braun multiplier is shown in the figure 11.

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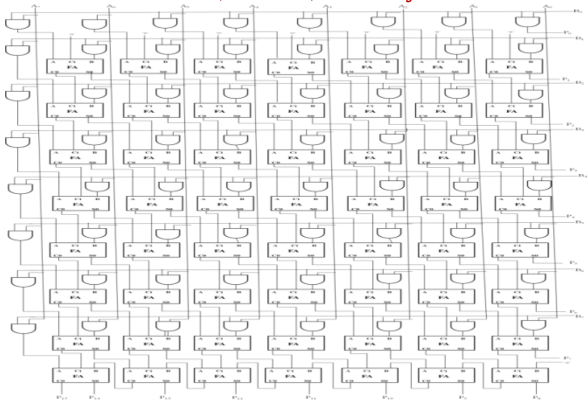

Fig 11 Schematic diagram of 8x8 Braun Multiplier

VII. WALLACE TREE MULTIPLIER USING COMPRESSORS

A. Wallace Tree Multiplier

The partial-sum adders can also be rearranged in a tree like fashion, reducing both the critical path and the number of adder cells needed.[9] The tree multiplier realizes substantial hardware savings for larger multipliers. The propagation delay is reduced as well. In fact, it can be shown that the propagation delay through the tree is equal to O (log3/2 (N)). While substantially faster than the carry-save structure for large multiplier word lengths, the Wallace multiplier has the disadvantage of being vary irregular, which complicates the task of an efficient layout design.

B. COMPRESSORS

Different Compressor logic based upon the concept of counter of full adder. Compressor is defined as single bit adder circuit that has more than three inputs as in full adder and less number of outputs.[7] Compressors can efficiently replace the combination of several half adders and full adders, thereby enabling high speed performance of the processor which incorporates the same. The schematics of 4:3, 5:3, 6:3,7:3 compressors are shown in the figures 12,13,14,15 respectively

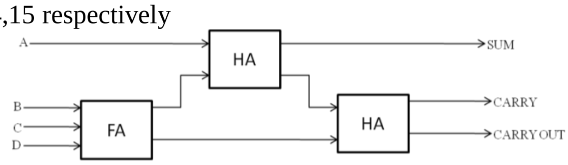

Fig 12 Schematic diagram of 4:3 compressor

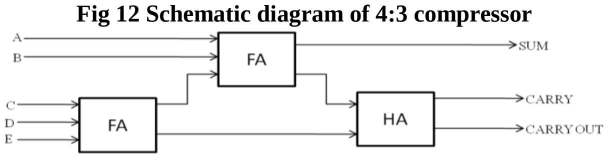

Fig 13 Schematic diagram of 5:3 compressor

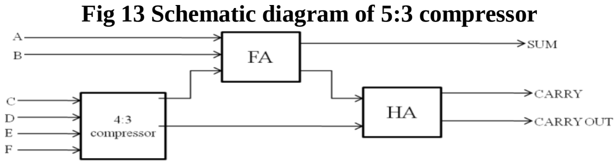

Fig 14 Schematic diagram of 6:3 compressor

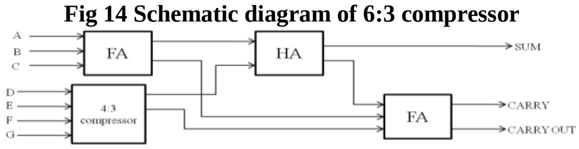

Fig 15 Schematic diagram of 7:3 compressor

The higher order compressors have been used intelligently so that the partial products are added in only two stages to obtain the final result and hence giving an area efficient and low power consuming design. Also, compressors and adders are employed such that minimum number of outputs is generated.[10] For example in column 5, there are 7 partial products to be added. These could be added using a 4-3 compressor and a full adder thereby generating five output bits. But instead of this a 7-3 compressor has been used which will generate only

3 output bits. The same approach has been utilized for other columns as well. The dot diagram of the Wallace tree multiplier using compressors is shown in figure 16

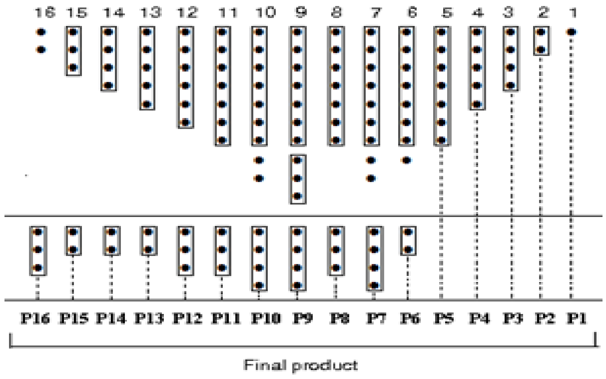

Fig 16 Dot diagram of the Wallace tree multiplier using compressors[9]

VIII. RESULTS

A. RTL schematics, input and output waveforms of 8-bit adders

The RTL schematics of 8-Bit Ripple Carry Adder, Carry Look Ahead Adder and SPST Adders are shown in the figures 17,18,19 respectively. The input and output waveforms are shown in the figure 5.4

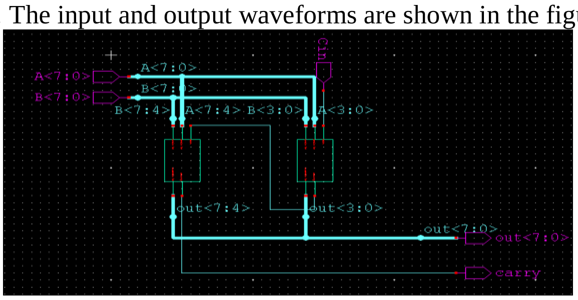

Fig 17: RTL Schematic of 8-bit Ripple Carry Adder

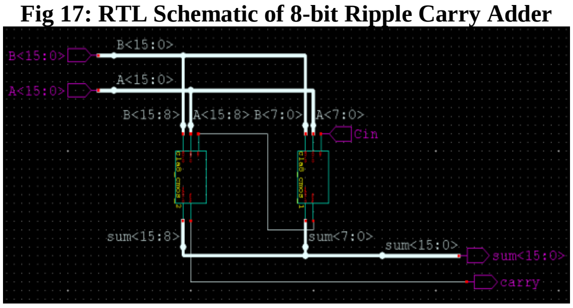

Fig 18: RTL Schematic of 8-bit Carry Look Ahead Adder

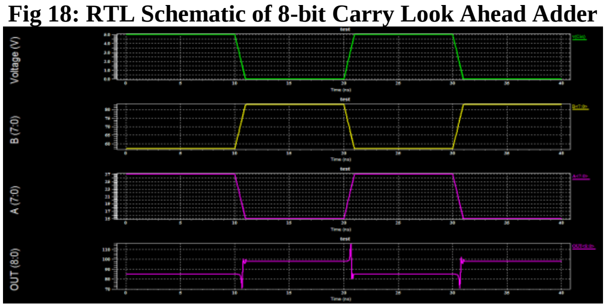

Fig 19: Input and Output Waveform of 8-bit Conventional Adder

B. RTL schematics, input and output waveforms of 8-bit parallel prefix adders

The RTL schematics of 8-Bit Kogge-Stone Adder, Brent-Kung Adder are shown in the figures 20,21 respectively. The input and output waveforms are shown in the figure 5.7

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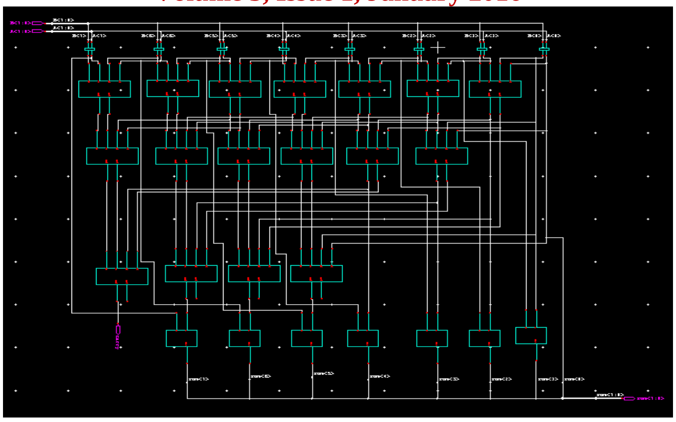

Fig 20: RTL Schematic of 8-bit Kogge-Stone Adder

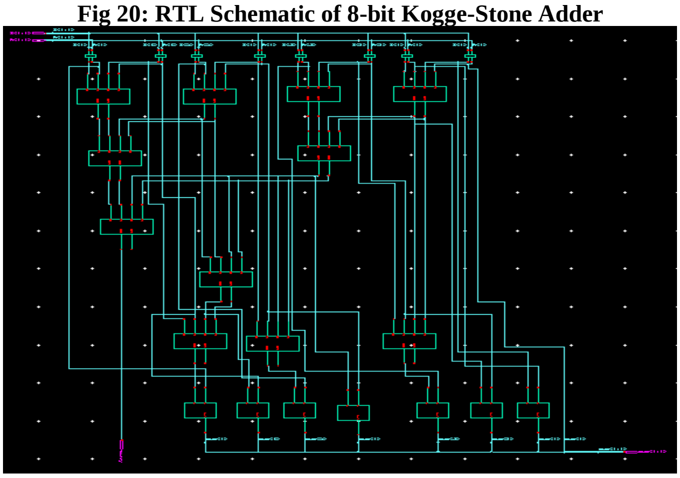

Fig 21: RTL Schematic of 8-bit Brent-Kung Adder

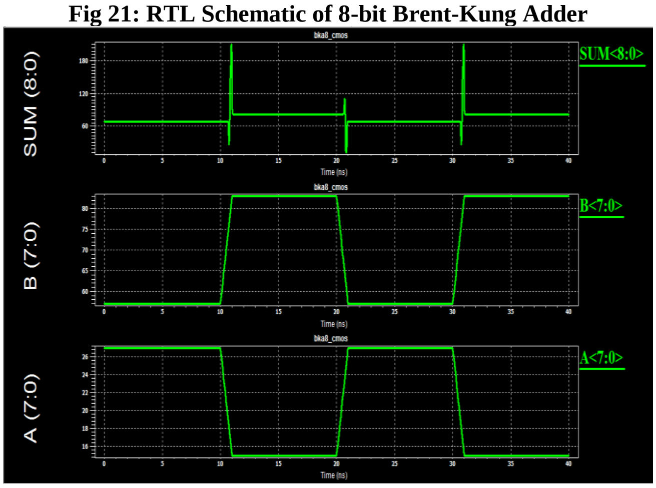

Fig 22: Input and Output Waveform of 8-bit Parallel Prefix Adder

C. RTL schematics, input and output waveforms of multipliers

The RTL schematics of 8-Bit Braun Multiplier and Wallace tree Multiplier using higher order compressors are shown in the figures 23,24 respectively. The input and output waveforms are shown in the figure 25

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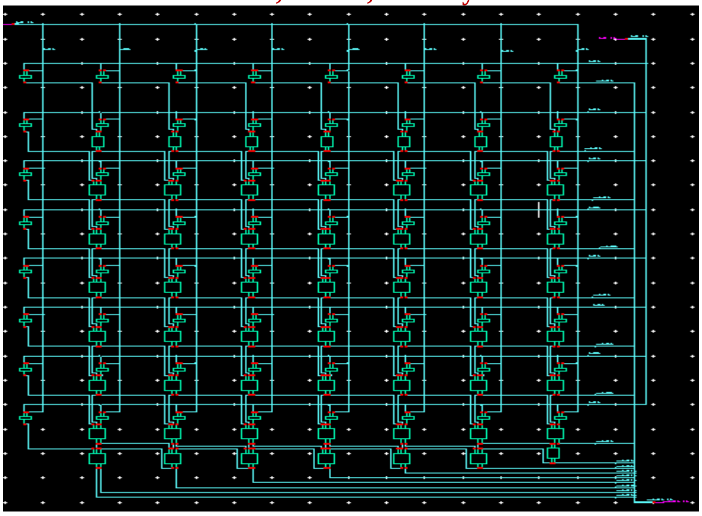

Fig 23: RTL Schematic of 8-bit Braun Multiplier

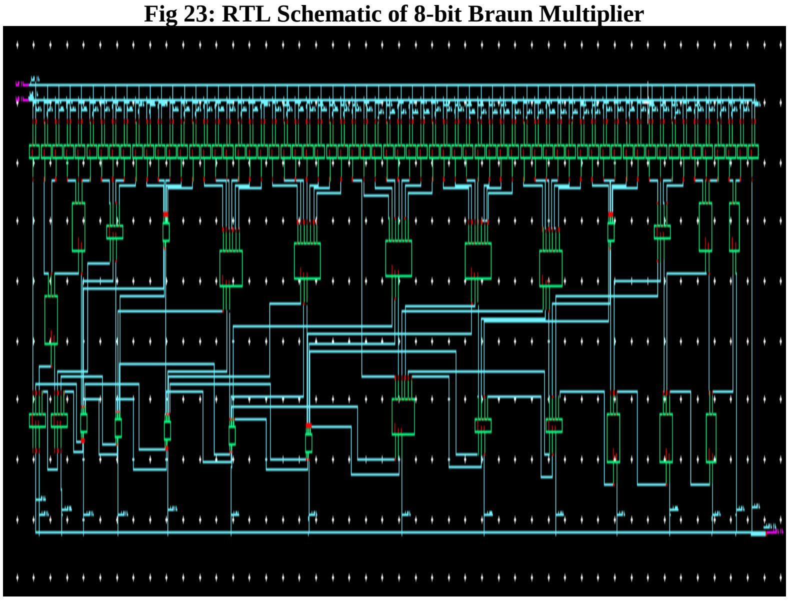

Fig 24: RTL Schematic of 8-bit Wallace tree multiplier using compressors

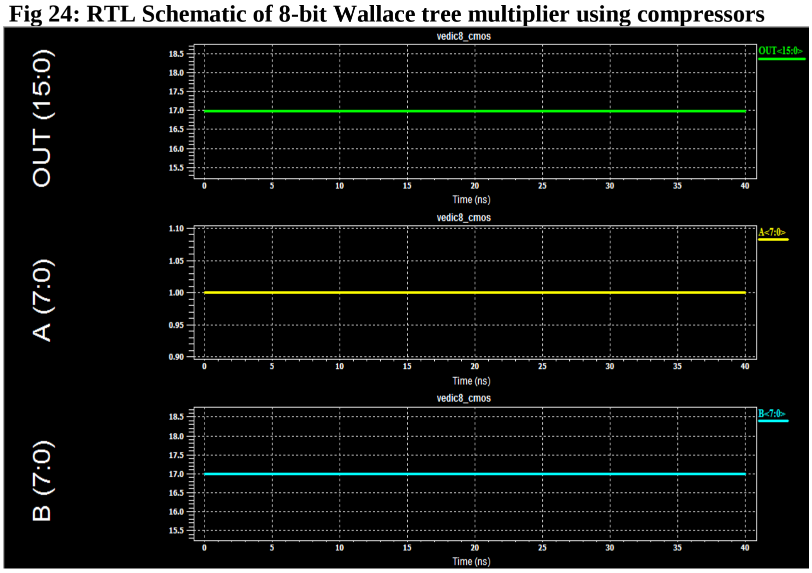

Fig 25: Input and Output Waveform of 8-bit Multiplier

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The Logic gates and Basic Modules, 8-bit Adders and Multipliers which are implemented in both CMOS and GDI logic are compared in terms of Power consumption; delay and no. of transistors are shown separately in the table 3

Table 3 Comparison of Logic gates and basic modules in both CMOS and GDI designs in terms of Power consumption, delay and no. of transistors

	Logic Gates and Basic Modules	Power Consumed		Time Delay		No. of Gates	
		CMOS(mWatts)	GDI(mWatts)	CMOS(sec)	GDI(sec)	CMOS	GDI
Logic Gates and Basic Modules	Nand gate	0.09235	0.1907	2.04	1.40	4	4
	Nor gate	0.07637	0.1231	1.86	1.49	4	4
	And gate	0.12236	0.00126	1.88	2.96	6	2
	Or gate	0.11197	0.0041	2.19	1.16	6	2
	Xor gate	0.24182	0.6099	2.47	1.23	14	4
	Half adder	0.24175	0.1457	1.91	1.11	14	6
	Full adder	0.60766	0.2285	2.03	2.76	34	10
Adders	Adders used	CMOS(mWatts)	GDI(mWatts)	CMOS(sec)	GDI(sec)	CMOS	GDI
	RCA	0.60859	0.121835	6.19	2.88	272	80
	CLA Adder	0.85214	0.10604	2.95	2.06	368	112
	KSA	1.2288	13.727	5.09	3.52	564	178
	BKA	0.93143	0.13837	4.78	2.91	456	142
Multipliers	Multipliers used	CMOS(mWatts)	GDI(mWatts)	CMOS(sec)	GDI(sec)	CMOS	GDI
	Braun Multiplier	4.6263	1.6315	7.86	1.93	2128	656
	WTM	5.5531	4.8732	10.42	5.29	2722	762

IX. CONCLUSION AND FUTURE WORK

In this work, different Adders like RCA, CLA Adder, KSA, BKA and different multipliers like Braun Multiplier and Wallace tree multipliers designed both in CMOS and GDI logics in Tanner tool. The results are compared in terms of power consumption, delay and number of transistors between CMOS logic designs and GDI logic designs. The results showed that when compared to CMOS logic based designs GDI logic based designs consumed 60% less power, 68% less delay and 80% less no. of Transistors. When the results are compared only in GDI logic. They showed that In Adders, CLA adder consumes less power, less delay and RCA consume less number of transistors. In Multipliers, Braun Multiplier consumes less power and Less delay and number of transistors.

In present work, the Adders and Multipliers are designed by using GDI. In future the work goes on designing ALU and MAC units and other applications of DSP by using the implemented Adders and Multipliers.

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