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Modified MAC based FIR Filter Using Carry Select Adders

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Abstract*— This paper used a regular and modified non linear carry select adders. In the regular and modified carry select adders, in the ripple carry adder section , the full adder is build with large number of exor , not and or gates. So a modification is done in case of this full adder. The full adder is build using 4:1 mux. So their will be large reduction in the delay. Then this carry select adder is used in the Wallace tree multiplier. Wallace tree multiplier is a combination of carry save addition and carry propagation addition. In the carry propagation addition ,we use this carry select adders. Now by using this multiplier and carry select adders, MAC based transpose FIR filtes are builded. And the simulation is done using XILINX ISE 14.7(VHDL).

***Index Terms*—CSLA, SQRT, MAC, FIR.**

I. INTRODUCTION

Design of area- and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position.The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum [1]. However,the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input Cin=0 and Cin=1 then the final sum and carry are selected by the multiplexers (mux).The basic idea of this work is to use Binary to Excess-1 Converter(BEC) instead of RCA with Cin=1 in the regular CSLA to achieve lower area and power consumption [2]–[4]. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure.

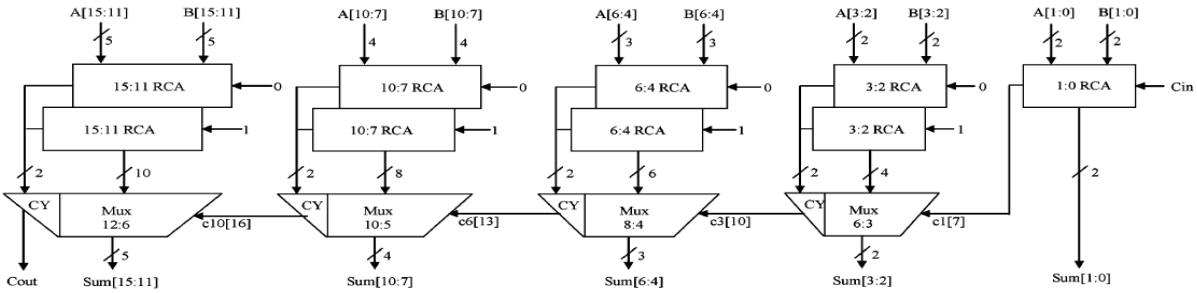

Fig. 1. Regular 16-b SQRT CSLA. [1]

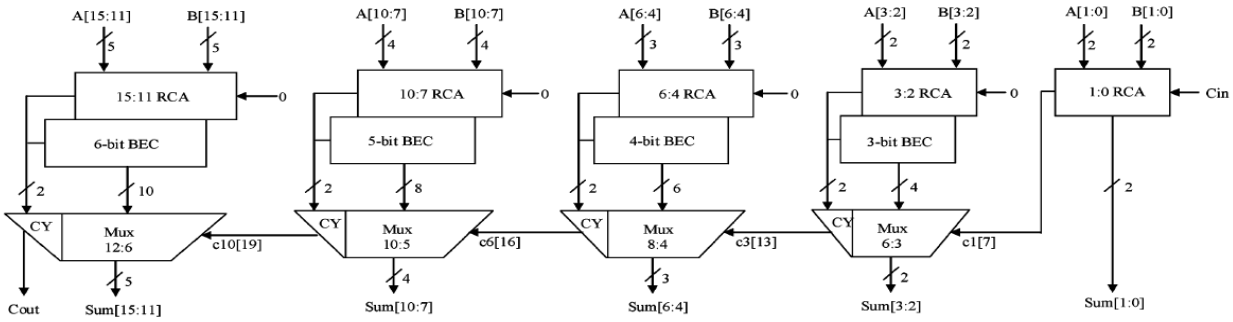

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Fig. 2. Modified 16-b SQRT CSLA. The parallel RCA with cin=1 is replaced with BEC.[1]

Carry select adder is used in Wallace tree multiplier .As wallace tree multiplier is a combination of carry save addition and carry propagate addition. In this case in the place of carry propagation we use regular and modified carry select adder. Here the full adder is build using XOR, AND, NOT and OR gates. Thus replacing that gates with 4:1 muxes will increase the speed. Then we use this multiplier and carry select adders for implementing the transposed FIR filter. This can be done using MAC unit.

II. LITERATURE REVIEW

Regular 16-bit carry select adder is having more area. Thus it can be reduced by using modified carry select adder. For that instead of using cin =1,in regular 16 bit square root carry select adder, it is replaced by a binary to excess-1 converter. Thus the area is reduced, but the delay is more. Thus both regular and modified carry select adder is having importance as one is having less area and one is having less delay. So for further reducing the delay the ripple carry adder is made using mux. As from reference [1] it is given that the full adder is made using large number of gates like XOR, AND, NOT and OR gates.

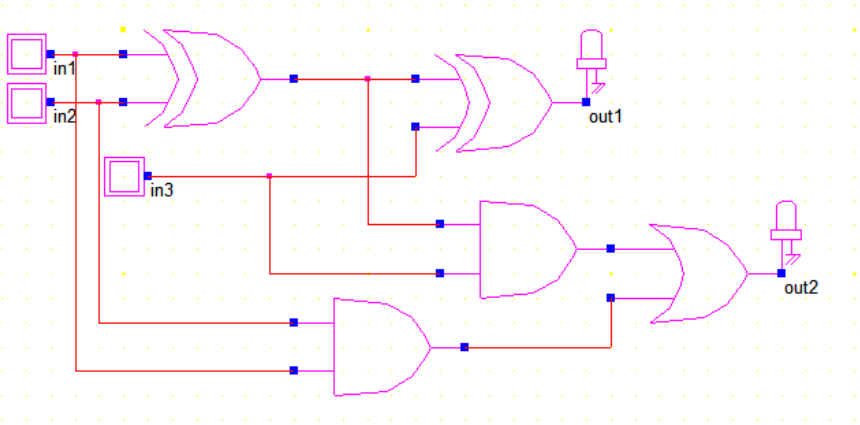

Fig.3.Fulladder without mux[1]

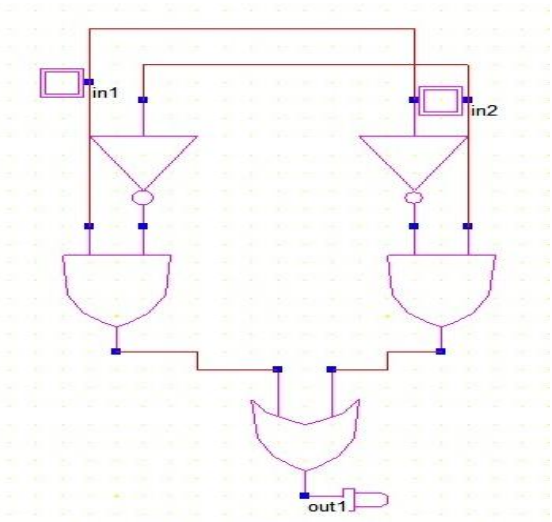

Fig.4.XOR gate[1]

So here full adder is made using two 4:1 muxes. Thus in the regular square root carry select adder, it is changed to a mux based regular square root carry select adder. And also it can be used in modified carry select adder. Then it is used in Wallace tree multiplier in the carry propagation stage. Then by using this multiplier and the adder, an FIR filter is implemented. For the simplicity in area and delay, a MAC unit is used for the implementation.

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III. CARRY SELECT ADDERS USING MUX

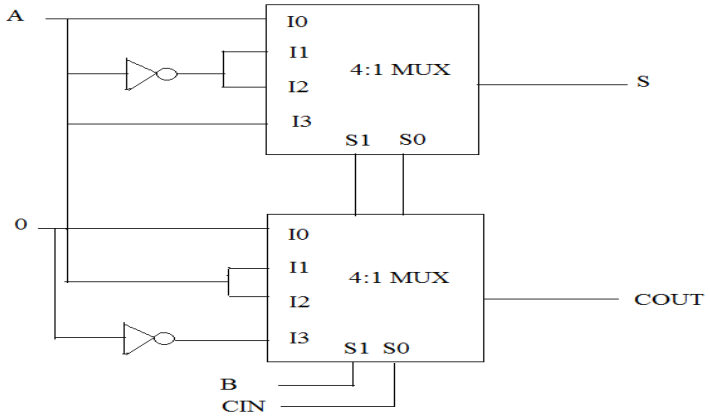

Fig.5.Fulladder using mux

Thus the whole carry select adder is changed to a mux based adder in case of regular 16 bit square root carry select adder.

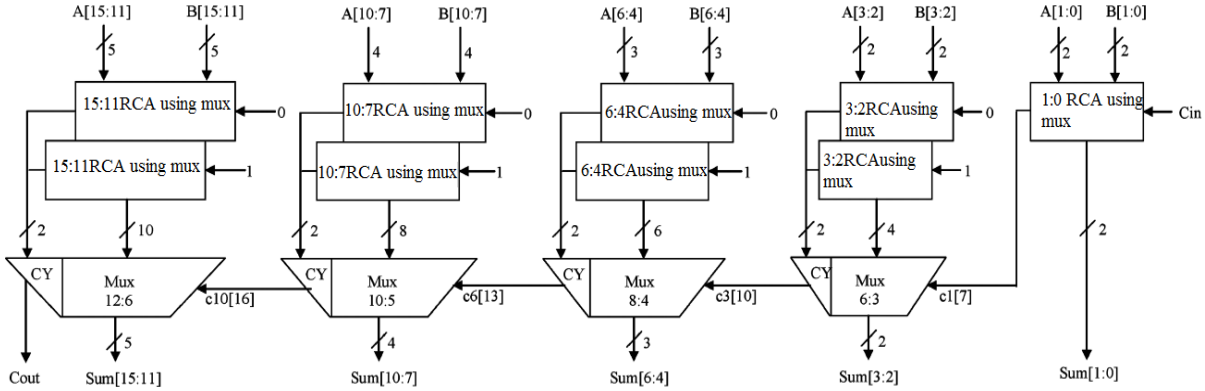

Fig.6.Regular carry select adder using mux

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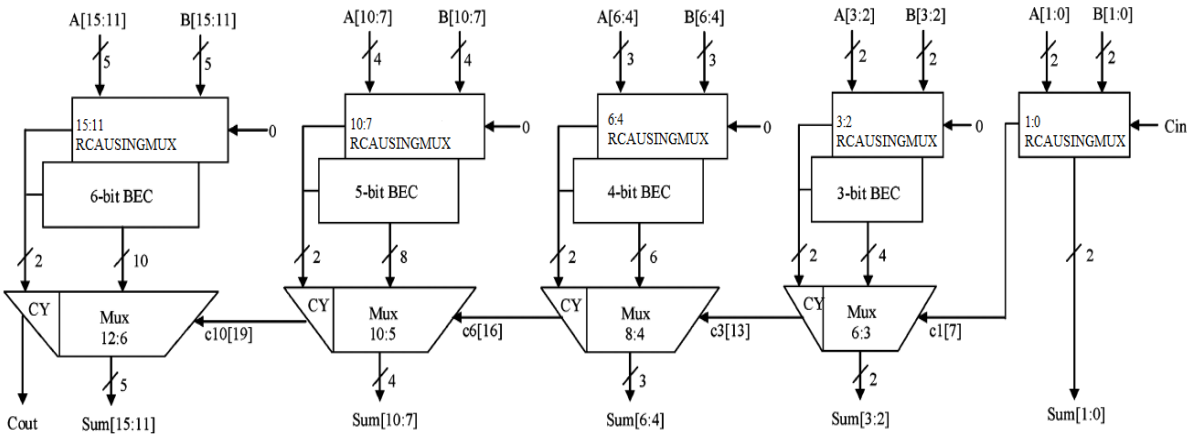

Fig.7.Modified carry select adder using mux

IV. FIR DIGITAL FILTER

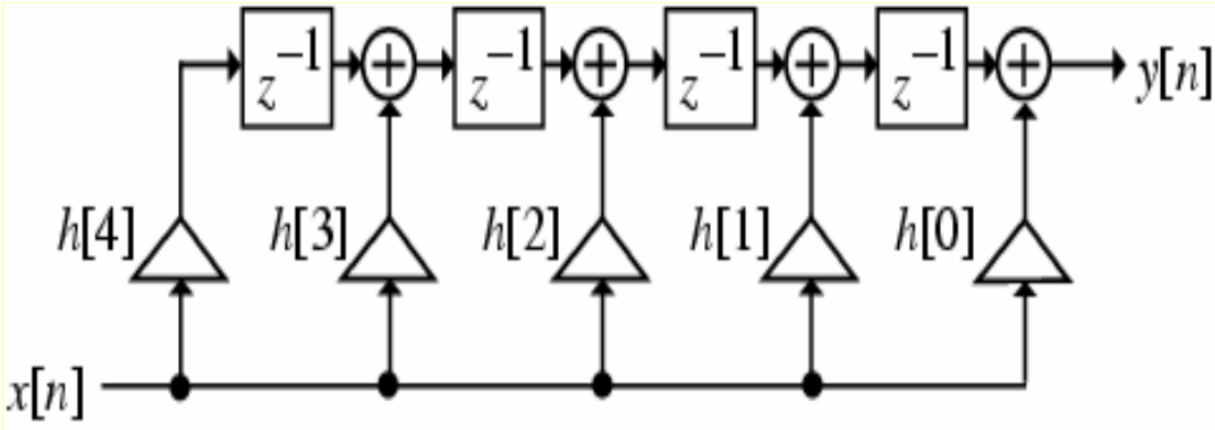

Fig 8.Transpose of 4 tap FIR digital filter

In signal processing, a finite impulse response (FIR) filter is a filter whose impulse response (or response to any finite length input) is of finite duration, because it settles to zero in finite time. This is in contrast to infinite impulse response (IIR) filters, which may have internal feedback and may continue to respond indefinitely (usually decaying).

The impulse response (that is, the output in response to a Kronecker delta input) of an Nth-order discrete-time FIR filter lasts exactly N + 1 samples (from first nonzero element through last nonzero element) before it then settles to zero.

FIR filters can be discrete-time or continuous-time, and digital or analog. The transposed form of the FIR filter produces the same output as the direct form. The difference is that it performs all the multiplications of a variable at the same time. The shift registers are moved to delay the output from a multiplication instead of the input. This way different algorithm can be applied to the FIR filter. The main advantage of using FIR filters is that an exact linear-phase response can be obtained. Here 4 tap FIR filter is used.4 tap means 4 delay unit.

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V. FIR DIGITAL FILTER USING CARRY SELECT ADDERS

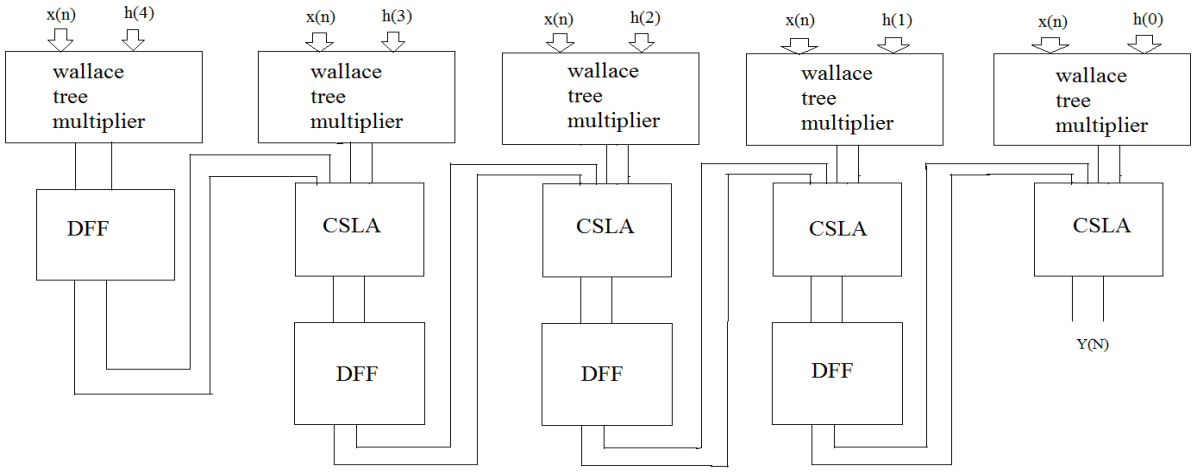

Fig.9. Transpose of 4 tap FIR digital filter using CSLA

Thus the fir filter uses multiplier as the Wallace tree multiplier, adder as the CSLA and the delay unit as the DFF. If we use this structure, entire area as well as delay will be more. Lot of time consumption will be there. Large number of adder, multiplier and dff are needed. Thus the entire structure as shown above can be replaced with a MAC (Multiply and Accumulate unit) unit.

VI. MAC UNIT

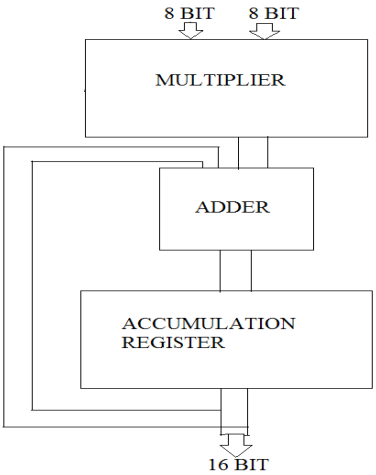

Fig.10.MAC UNIT

In computing, especially digital signal processing, the multiply–accumulate operation is a common step that computes the product of two numbers and adds that product to an accumulator. The hardware unit that performs the operation is known as a multiplier–accumulator (MAC, or MAC unit); the operation itself is also often called a MAC or a MAC operation. The MAC operation modifies an accumulator a:a+(b*c)

When done with floating point numbers, it might be performed with two roundings (typical in many DSPs), or with a single rounding. When performed with a single rounding, it is called a fused multiply–add (FMA) or fused multiply–accumulate (FMAC).

Modern computers may contain a dedicated MAC, consisting of a multiplier implemented in combinational logic followed by an adder and an accumulator register that stores the result. The output of the register is fed back to one input of the adder, so that on each clock cycle, the output of the multiplier is added to the register. Combinational

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multipliers require a large amount of logic, but can compute a product much more quickly than the method of shifting and adding typical of earlier computers. The first processors to be equipped with MAC units were digital signal processors, but the technique is now also common in general-purpose processors.

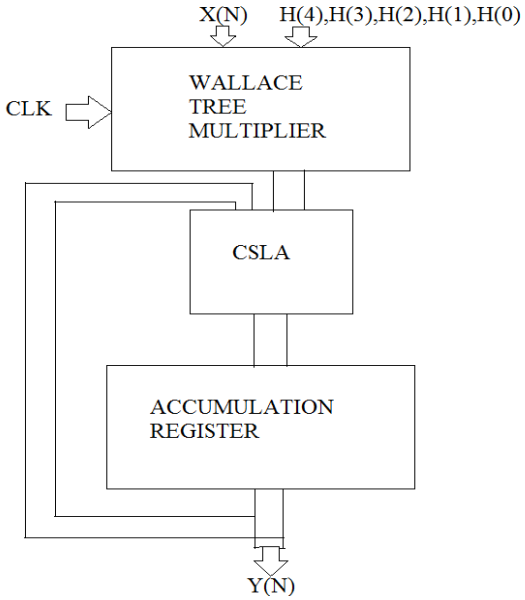

Fig.11.Modified MAC based FIR filter

Thus in here instead of multiplier stage we use Wallace tree multiplier, adder stage we use carry select adders and in the accumulation register we use PIPO register. This PIPO register is used to store data. Parallel In Parallel Out register uses D flip flop. Thus this PIPO will be acting as the delay unit when considering filter.

TABLE I. COMPARISON OF ADDERS

ADDER	DELAY(ns)
REGULAR CSLA	17.503
REGULAR CSLA USING MUX	16.401
MODIFIED CSLA	21.848
MODIFIED CSLA USING MUX	21.816

TABLE II.COMPARISON OF MULTIPLIERS

MULTIPLIER	DELAY(ns)
WALLACE TREE MULTIPLIER USING REG CSLA	26.868
WALLACE TREE MULTIPLIER USING MUX BASED REG CSLA	24.085
WALLACE TREE MULTIPLIER USING MOD CSLA	27.303
WALLACE TREE MULTIPLIER USING MUX BASED MOD CSLA	26.813

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VII. SIMULATION

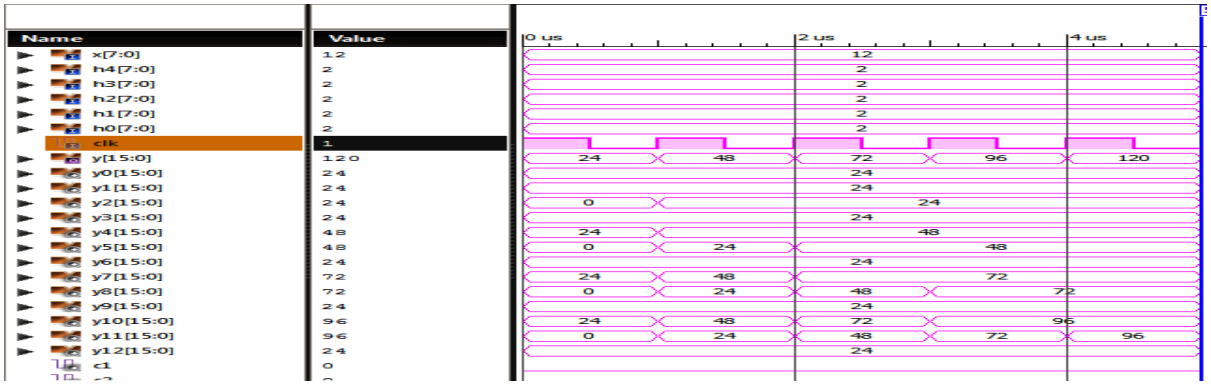

Fig.12.Modified MAC based 4 tap FIR filter

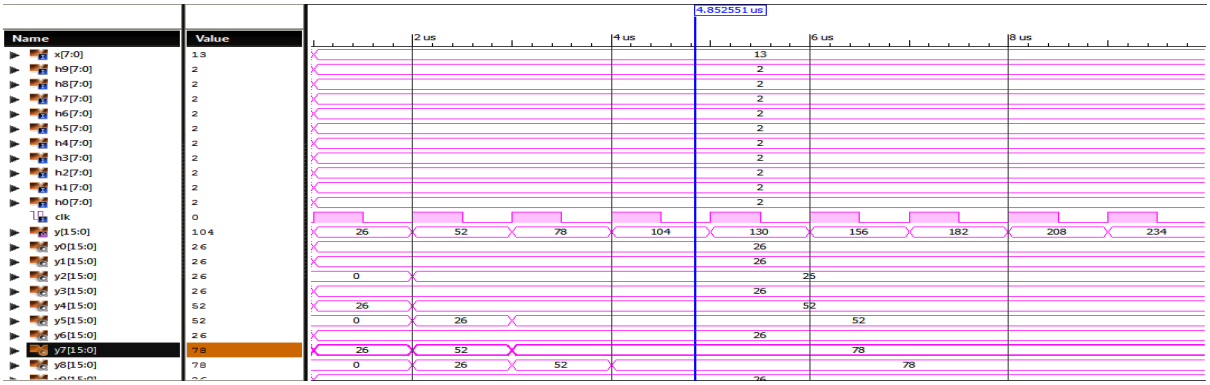

Fig.13.Modified MAC based 8 tap FIR filter

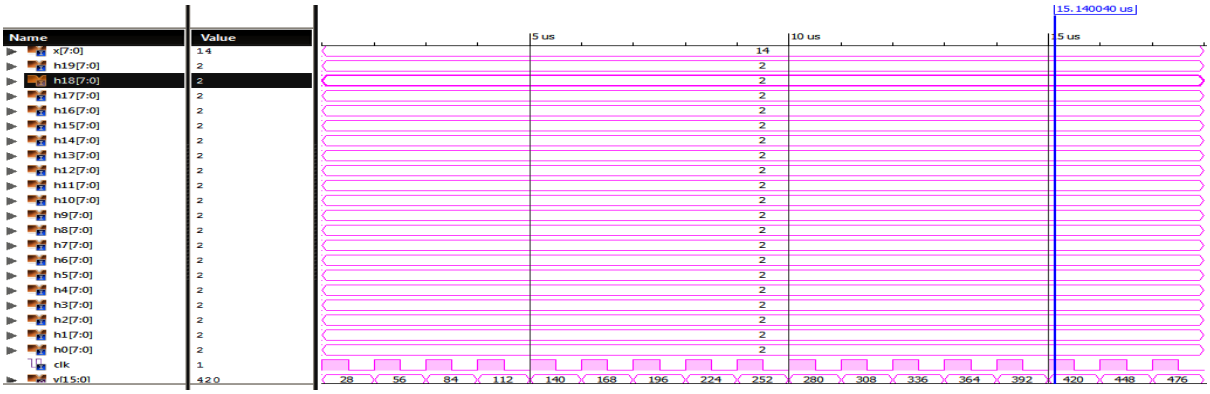

Fig.14.Modified MAC based 16 tap FIR filter

VIII. CONCLUSION

This Paper is based on a nonlinear regular and modified carry select adders .Thus giving a modification in the ripple carry adder stage can reduce the delay more. And by using this, the regular carry select adder is changed to a mux based carry select adder. This can be used in the carry propagation stage of Wallace tree multiplier. And by using this multiplier and mux based regular carry select adder, a MAC based FIR filter is implemented. Here 4 tap,8 tap and 16 tap FIR filter is implemented. More tap means more stop band attenuation, less ripple, narrower filters can be obtained. This filters can be used in image processing, DSP processors etc.

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