ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 4, Issue 3, May 2015

A Survey of Design and Implementation of High Speed Carry Select Adder

SWATI THAKUR, SWATI KAPOOR

Abstract*— This paper represent the reviewing of different existing techniques of designing the carry select adder. Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions .CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carriers and then select a carry to generate the sum. From the structure of CSLA we can see that there is scope of reducing, area, delay. and power consumption. In this paper three previous existing techniques are reviewed .First technique is CSLA with ripple carry adder, CSLA with BEC & the third technique is CSLA with D- latch .We are comparing these three existing techniques in terms of area, delay and power consumption for conventional fast adder architecture to prove its efficiency.

***Index Term*— Literature Survey, Conventional Adder Circuits, RCA, BEC, D-Latch.**

I. INTRODUCTION

Adders have a special significance in VLSI designs and it is used in computer and many other processor to perform the arithmetic functions. It is used to calculate addresses, table indices and similar applications. High speed addition and multiplication has always been a fundamental requirement of high-performance processors and systems in VLSI. Now a day design of low power and area efficient high speed data path logic systems are most substantial area in the research of VLSI design. Number of fast adders can be used for addition. In digital adders the sum of each bit position is added and the generated carry is propagated into the next position. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. There are many adders in digital system. Out of these adders CSLA is the fastest adder. The regular method of designing a CSLA is using ripple carry adder (RCA). However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input CIN = 0 and CIN = 1, then the final sum and carry are selected by the multiplexers (mux).

To overcome the above problem of area a new method was introduced. CSLA with the n-bit binary to excess-1 code converters (BEC) to improve the speed of addition. This logic can be replaced in RCA for Cin=1 to further improves the speed and thus reduces the delay. Using Binary to Excess -1 Converter (BEC) instead of RCA in the regular CSLA will achieve lower area, delay which speeds up the addition operation. The main advantage of this BEC logic comes from the lesser number of logic gates than the Full Adder (FA) structure because the number of gates used will be decrease. But this technique results in increasing the delay of the circuit. Now to overcome the problem of delay a new technique was introduced .CSLA with D-latch. This architecture replaces the BEC by D-latch with enable signal. This method reduces the area, delay and power. Therefore the main aim of the paper is to design and implement a high speed carry select adder to enhance the speed of addition and perform fast arithmetic function.

II. LITERATURE REVIEW

In 1962, O.J.Bedrij [1] described the extremely fast digital adder with sum selection and multiple-radix carry. He compared the amount of hardware and the logical delay for a 100-bit ripple-carry adder and a carry-select adder. The problem of carry-propagation delay was overcome by independently generating multiple-radix carries and using these carries to select between simultaneously generated sums. In this adder system, the addend and augend were divided into sub addend and sub augend sections that were added twice to produce two sub sums. One addition was done with a carry digit forced into each section, and the other addition combined the operands without the forced carry digit. The selection of the correct sub sum from each of the adder sections depended upon whether or not there actually was a carry into that adder section.

T.Y.Chang and M.J.Hsiao [3], suggested that instead of using dual ripple carry adders, a carry select adder scheme using an add one circuit to replace one ripple carry adder requires 29.2% fewer transistors with a speed

ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 4, Issue 3, May 2015

penalty of 5.9% for bit length n=64. If speed was important for this 64 bit adder, then two of carry-select adder blocks could be substituted by the proposed scheme with a 6.3% area saving and the same speed.

The B.Ramkumar, H.M.Kittur, and P. M. Kannan in 2010 [3] suggested a very simple approach to improve the speed of addition. Based on this approach a 16, 32 and 64-bit adder architecture was developed and compared with conventional fast adder architectures. In many parallel multipliers to speed up the final addition, CLA was arranged in the form of Carry Select adder (CSLA) & was used. But due to the structure of the CSLA it occupied more chip area, because it uses multiple pairs of RCA's to generate the partial sum and carry by considering Cin=0 and Cin=1.Thus the complexity of the final adder structure was high. So they replaced the RCA (CLA) with Cin=1 with BEC logic, which reduced the maximum area but delay is increased in the final adder structure.

Ramkumar and Harish 2011 [4] propose BEC technique which is a simple and efficient gate level modification to significantly reduce the area and power of square root CSLA.
Veena nair in 2013 suggested a new approach in with D-latch is used with enabled signal instead of BEC [6]. Based on this approach a 16, 32 and 64-bit adder architecture was developed and compared with conventional fast adder architectures .The new structure as a result reduces the delay of the structure.

III. 16-BIT REGULAR CARRY SELECT ADDER

A Carry Select Adder is a particular way to implement an adder, which is a logic element that computes the (n+1) bit sum of two n-bit numbers. The carry-select adder is simple but rather fast. The carry-select adder generally consists of two ripple carry adders and a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known [2].

Ripple Carry Adder

The ripple carry adder is constructed by cascading full adders (FA) blocks in series. One full adder is responsible for the addition of two binary digits at any stage of the ripple carry. The carryout of one stage is fed directly to the carry in of the next stage.4-Bit ripple carry adder. A serious drawback of this adder is that the delay increases linearly with the bit length.The structure of a 16 bit CSLA is shown below:

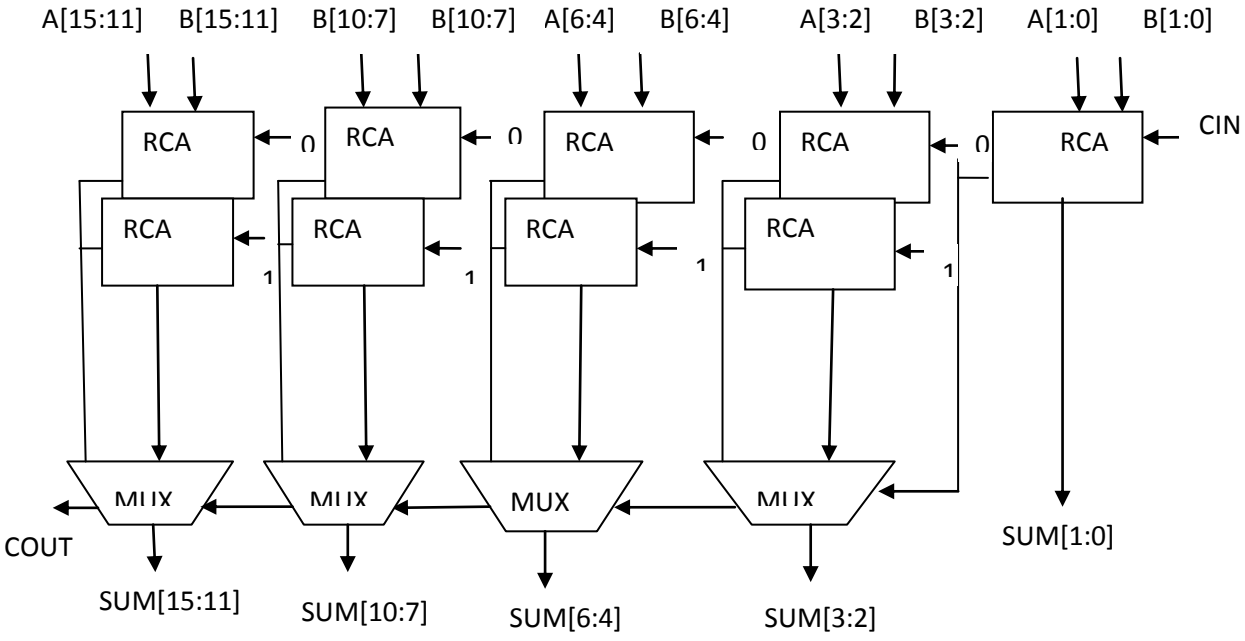

FIG. 1 16-BIT REGULAR CSLA

ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 4, Issue 3, May 2015

A carry-select adder is divided into sectors, each of which, except for the least significant performs two additions in parallel, one assuming a carry-in of zero, the other a carry-in of one within the sector, there are two 4-bit ripple carry adders receiving the same data inputs but different Cin. The upper adder has a carry in of zero, the lower adder a carry-in of one. The actual Cin from the preceding sector selects one of the two adders. If the carry-in is zero, the sum and carry-out of the upper adder are selected. If the carry-in is one, the sum and carry-out of the lower adder are selected [2]. Logically, the result is not different if a single ripple-carry adder were used. Then 2, 3, 4, 5-bit ripple carry adder was done by calling the full adder. The regular 16- bit CSLA was created by calling the ripple carry adders and all multiplexers based on circuit. It has five groups of different size RCA. The delay and area of each group has to be evaluated. To do this, we first need to evaluate the delay and area of each of the basic adder blocks used in the structure of the CSLA. The source code is written for all the above adder blocks like Xor gate, half adder, full adder, multiplier, ripple carry adder and finally the Regular carry select adder using VHDL. Simulation will be done to verify the functionality and synthesis will be done to get the NETLIST using Xilinx ISE.

IV. CARRY SELECT ADDER WITH BINARY TO EXCESS ONE CONVERTER (BEC)

The regular CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input and then the final sum and carry are selected by the multiplexers (mux). To overcome the above problem, the regular CSLA is modified by using n-bit Binary to Excess-1 code converters (BEC) to improve the speed of addition [4]. The Binary to excess one Converter (BEC) replaces the ripple carry adder with Cin=1, in order to reduce the area and power consumption of the regular CSLA. The structure is again divided into five groups with different bit size RCA and BEC. One input to the mux goes from the RCA with Cin=0 and other input from the BEC. This logic can be implemented with any type of adder to further improve the speed. The below Fig. 2 shows the structure of modified carry select adder.

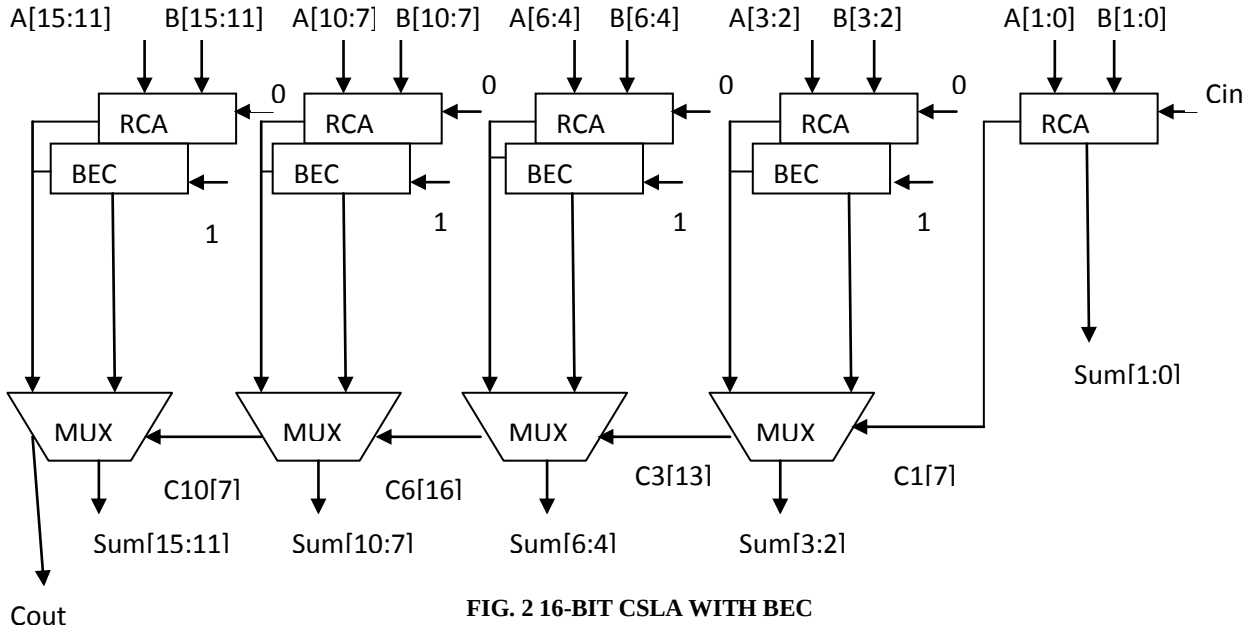

FIG. 2 16-BIT CSLA WITH BEC

Binary To Excess-1 Converter

The basic idea of this modified work is to use Binary to Excess-1 Converter (BEC) instead of RCA with Cin=1 in the regular CSLA to achieve lower area and power consumption with only a slight increase in the delay [2] [3]. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure.

ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 4, Issue 3, May 2015

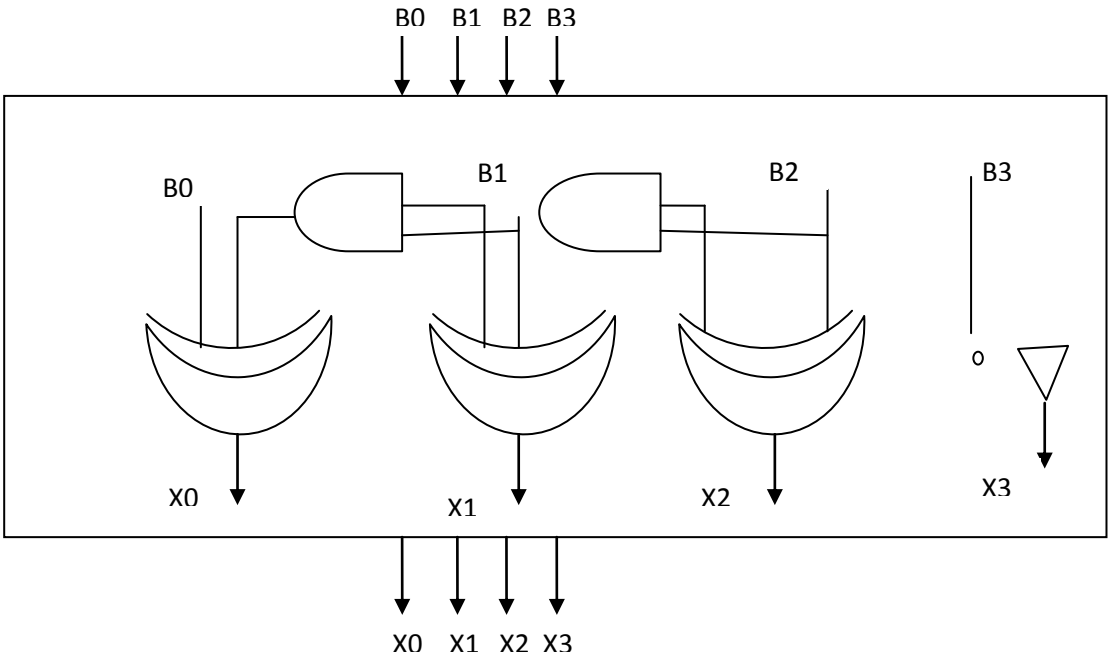

FIG. 3 4-BIT BEC

Here again the simulation and synthesis is performed using Xilinx ISE and the results are compared with the Regular CSLA.

V. CARRY SELECT ADDER WITH D-LATCH:

When the modified CSLA is simulated and synthesized, the area and power is less in the CSLA with BEC but the delay is slightly increased. So we can improve the above structure in terms of less delay and higher speed by replacing the BEC with a D-Latch. Thus an improved Carry Select Adder with D-Latch is shown below.

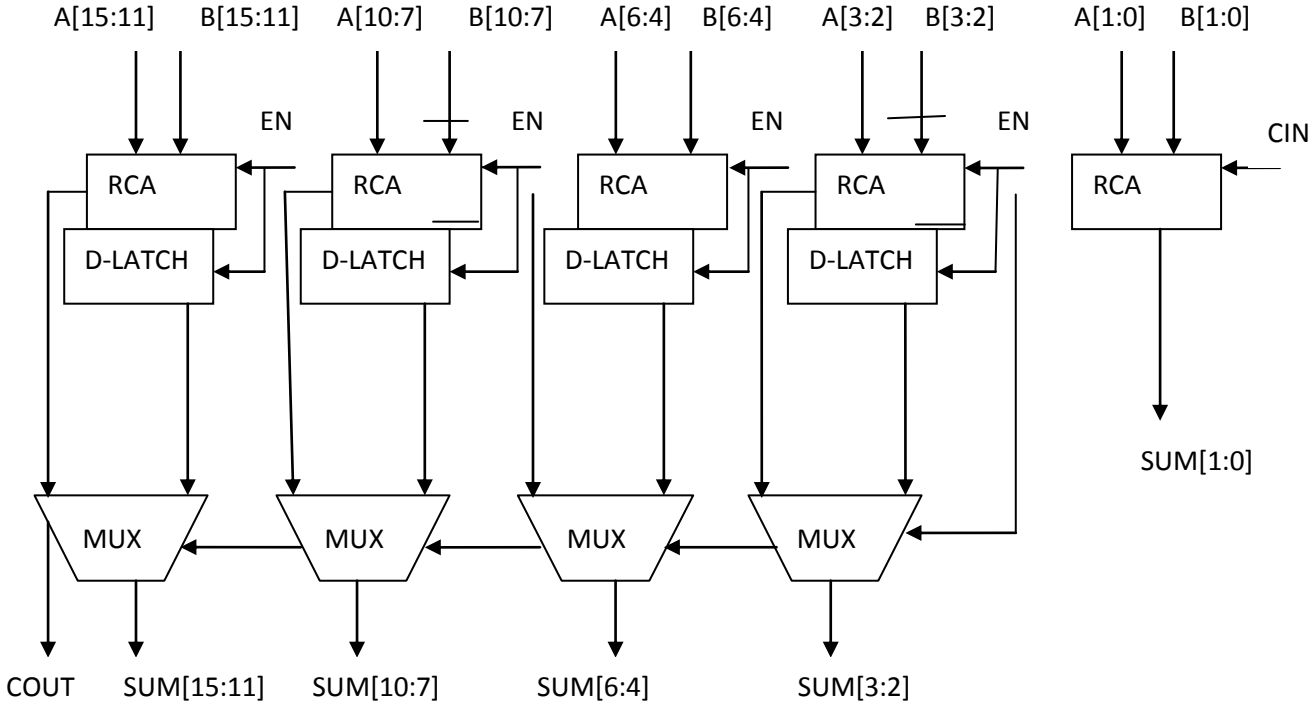

FIG. 4 16-BIT MODIFIED CSLA WITH D- LATCH

ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 4, Issue 3, May 2015

This method replaces the BEC add one circuit by D-latch with enable signal. Latches are used to store one bit information. Their outputs are constantly affected by their inputs as long as the enable signal is asserted. In other words, when they are enabled, their content changes immediately according to their inputs [4]. The architecture of proposed 16-b CSLA is shown in Fig. 4. It has different five groups of different bit size RCA and D-Latch. Instead of using two separate adders in the regular CSLA, in this method only one adder is used to reduce the area, power consumption and delay. Each of the two additions is performed in one clock cycle. This is 16-bit adder in which least significant bit (LSB) adder is ripple carry adder, which is 2 bit wide. The upper half of the adder i.e, most significant part is 14-bit wide which works according to the clock. Whenever clock goes high addition for carry input one is performed. When clock goes low then carry input is assumed as zero and sum is stored in adder itself. From the Fig. it can understand that latch is used to store the sum and carry for Cin=1 and cin=0.Carry out from the previous stage i.e, least significant bit adder is used as control signal for multiplexer to select final output carry and sum of the 16-bit adder. If the actual carry input is one, then computed sum and carry latch is accessed and for carry input zero MSB adder is accessed. Cout is the output carry [5].

VI. COMPARISON OF DIFFERENT TEHNIQUES OF CSLA:

BIT SIZE	TYPE OF ADDER	DELAY(ns)	AREA(nm)	POWER(mw)	POWER DELAY PRODUCT(10^ -12)
	REGULAR CSLA	2.195	955.937	15.241	33.45
8 BIT	BEC CSLA	3.336	628.906	14.229	49.46
	WITHOUT MUX	3.337	434.843	7.956	26.55
	USING D-LATCH	2.094	952.343	13.598	28.47

TABLE 1: 8-BIT RESULTS COMPARISON

When compared to regular and modified circuit delay is reduced but power and area is increased negligibly when compared to modified CSLA without using mux only.

BIT SIZE	TYPE OF ADDER	DELAY(ns)	AREA(nm)	POWER(mw)	POWER DELAY PRODUCT(10^ -12)
	REGULAR CSLA	4.848	2016.093	35.631	172.73
16 BIT	BEC CSLA	3.941	1362.031	33.458	131.793
	WITHOUT MUX	6.201	952.343	18.413	114.14
	USING D-LATCH	2.458	1901.093	29.311	71.80

TABLE 2: 16-BIT RESULTS COMPARISON

When compared to regular and modified circuit delay is reduced but power is increased when compared to modified CSLA without using mux. But here the power delay product and area delay product is reduced when compared to regular and modified circuit.

BIT SIZE	TYPE OF ADDER	DELAY(ns)	AREA(nm)	POWER(mw)	POWER DELAY PRODUCT(10^ -12)
	REGULAR CSLA	6.587	4161.562	77.499	510.48
64 BIT	BEC CSLA	6.729	2813.906	71.499	480.78
	WITHOUT MUX	9.539	1958.593	39.0177	372.18
	USING D-LATCH	3.655	3856.693	61.407	224.41

TABLE 3: 32-BIT RESULTS COMPARISON

When compared to regular and modified circuit delay is reduced but power is increased when compared to modified CSLA without using mux. But here the power delay product and area delay product is reduced when compared to regular and modified circuit.

ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 4, Issue 3, May 2015

VII. CONCLUSION

In this paper, various types of Carry select adder design have been reviewed from the most recent and previous published research work. Various different logics are used in this paper to build the carry select adder to reduce the power, delay, area and power-delay product and transistors count. Based on survey it is conclude that the CSLA with ripple carry adder is not area efficient so modified CSLA with BEC-1 had been introduced which consume less power and area with slightly increase in the delay the power delay product and area-delay product have also decrease for 16, 32, 64-bit sizes which indicated the success of the method and not a mere trade off of delay for power and area. So, to remove the problem of delay a new CSLA with D-latch is introduced. This modified CSLA architecture is therefore low power, low area, simple and efficient for VLSI application. Therefore the total power consumption, area and delay will be reduced which gives the high speed addition operation and good performance of the system.

ACKNOWLEDGMENT

The authors thank the Management and Vice Chancellor of Bahra University Shimla Hills for providing excellent computing facility and encouragement for the completion of this work

REFERENCES

[1] O. J. Bedrij, "Carry-select adder," IRE Trans. Electron. Comput., pp.340–344, 1962.

[2] T. Y. Ceiang and M. J. Hsiao, "Carry-select adder using single ripple carry adder," Electron. Lett., vol. 34, no. 22, pp. 2101–2103, Oct. 1998.

[3] N Dhanunjaya Rao, "Design and Implementation of High Speed Carry Select Adder International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE) – Volume 1, Issue 6, December 2012.

[4] B. Ramkumar, H.M. Kittur, and P. M. Kannan, "ASIC Implementation Of Modified Faster Carry Save Adder," Eur. J. Sci. Res., vol. 42, no. 1, pp. 53–58, 2010.

[5] B. Ramkumar and Harish M Kittur "Low-Power and Area-Efficient Carry Select Adder" IEEE Trans. on very large scale integration systems 2012.

[6] B.Gopinath1, N.Sangeetha, S.Jenifer Nancy and T.Umarani "Design and Implementation of High Speed Carry Select Adder" International Journal of Engineering Research & Technology (IJERT), Vol. 4 Issue 02, February-2015.

[7] Veena V Nair, "Modified Low-Power and Area-Efficient Carry Select Adder using D-Latch '"International Journal of Engineering Science and Innovative Technology (IJESIT) Volume 2, Issue 4, July 2013

AUTHOR BIOGRAPHY

Swati thakur was born in hamirpur, himachal Pradesh, India. She has received her B.Tech degree in Electronics and Communication Engineering from Himachal Pradesh University Shimla, India and pursuing M. Tech in from Electronics and communication from bahra university Shimla hills, India. Currently she is a student in from bahra university Shimla hills, India.