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Implementation and Performance Comparison of Modified Booth Multiplier by using Different Adder Techniques

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Abstract*—The multiplication operation is present in many parts of a digital system or digital computer, most in Digital signal processing, graphics and scientific computation. With advances in technology, various techniques have been proposed to design multipliers, which offer high speed, low power consumption and lesser area. In this paper modified booth multiplier (radix-4) is implemented in Verilog and performance parameters like area, path delay, fan-out, speed of multiplier are compared using different adder techniques. Modified booth encoder is used to generate the partial products and these are half compared to that of normal multiplication by using modified booth algorithm. These products are added by using various adders and produces the final product of multiplication. The adders used in this paper are Ripple carry adder, carry look ahead adder, and carry select adder, kogge-stone adder and sparse kogge-stone adder.

***Index Terms*— Booth Encoder, Carry select adder, Carry look ahead adder, Koggestone adder, Modified Booth Multiplier, Partial product, Ripple carry adder, Sparse koggestone adder.**

I. INTRODUCTION

Multiplication is an important fundamental function in arithmetic logic operation. Since, multiplication dominates the execution time of most DSP algorithms; therefore, high-speed multiplier is much desired. Various algorithms proposed for multiplication are Booth Algorithm, Modified Booth Algorithm. Booth's multiplication algorithm is a multiplication algorithm that multiplies two signed binary numbers in two's complement notation. In this paper use of different adders like Carry select adder, Carry look ahead adder, Koggestone adder, Ripple Carry adder and sparse koggestone adder, technique for enhancing the performance and reducing the area of modified booth multiplier.

Fast multipliers are essential parts of digital signal processing systems. The speed of multiply operation is of great importance in digital signal processing as well as in the general purpose processors today, especially since the media processing took off. In the past multiplication was generally implemented via a sequence of addition, subtraction, and shift operations. Multiplication can be considered as a series of repeated additions. The number to be added is the multiplicand, the number of times that it is added is the multiplier, and the result is the product[1]. Each step of addition generates a partial product. In most computers, the operand usually contains the same number of bits. When the operands are interpreted as integers, the product is generally twice the length of operands in order to preserve the information content. This repeated addition method that is suggested by the arithmetic definition is slow that it is almost always replaced by an algorithm that makes use of positional representation. It is possible to decompose multipliers into two parts. The first part is dedicated to the generation of partial products, and the second one collects and adds them. The addition of partial products is done by using different adders in Modified Booth Multiplication. The block diagram of modified booth multiplier is shown in Figure 1.The block diagram consist of modified booth encoder, partial product generator and different types of adders for generating the product [1].

II. SYSTEM OVERVIEW

The block diagram of modified booth multiplier is shown in Figure 1.The block diagram consist of modified booth encoder, partial product generator and different types of adders for generating the product. Functionality of each block is described.

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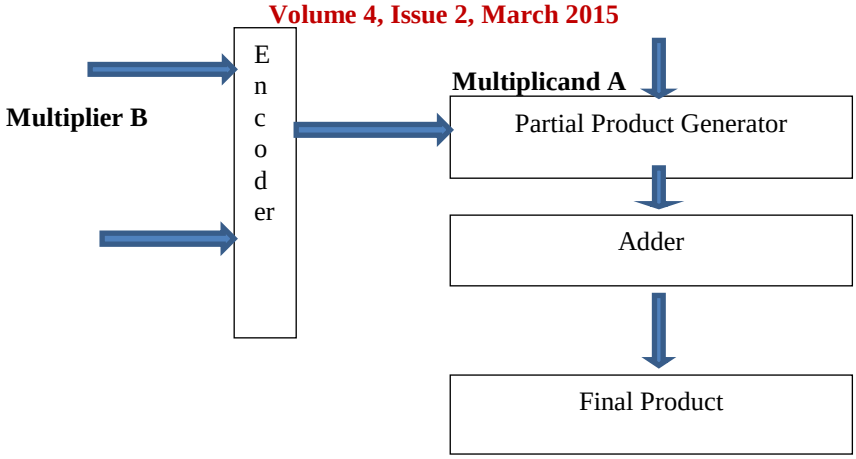

Fig 1: Block Diagram of Modified Booth Multiplier

a) MODIFIED BOOTH ENCODER

The Modified Booth's Algorithm (MBA) Radix-4 is used for high speed multiplication [2],[3]. This type of multiplier operates much faster than an array multiplier because its computation time is proportional to the logarithm of the word length of operands. Advantage of this method reduced the partial product by half. It recode the multiplier term. It recodes the block of three bits, such that each block overlaps the previous block by one bit. In starting grouping from LSB, it contains the two bit of the multiplier and one additional LSB bit of first block assumes to be '0'.

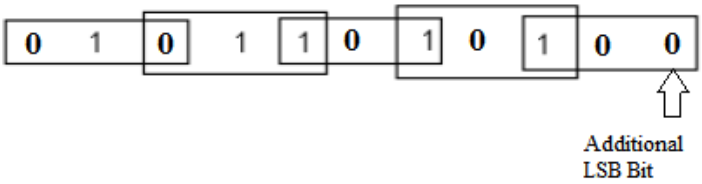

Fig 2: Grouping of bits of the multiplier

Figure 2 shows the grouping of bits of the multiplier 'B' term for use of Booth Encoding. Each block of multiplier is decoded to generate the partial products. According to the encoding algorithm generates five signed digits 0,-1,-2,+1,+2. These encoded digits perform operation with the multiplicand term and generates the partial products as shown in Table 1.

Table. I: Booth-4 Encoding

Block (Multiplier bits)	Re-coded Digit	Operation on Multiplicand
000	0	0A
001	+1	+1A
010	+1	+1A
011	+2	+2A
100	-2	-2A
101	-1	-1A
110	-1	-1A
111	0	0A

b) ADDERS

Addition is the fundamental operation in a multiplication process. In modified booth multiplication we use five types of adders for adding partial products and compare its performance parameters like area, fanout, speed of multiplication, maximum path delay etc. The five adders used are Ripple carry adder, Carry select adder, Carry look ahead adder, Koggestone adder, sparse koggestone adder.

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Ripple Carry Adder

The ripple carry adder is constructed by cascading full adders (FA) blocks in series. The carryout of one stage is given directly to the carry-in of the next stage. The number of full adders may be added to the ripple carry adder or ripple carry adders of different sizes may be cascaded in order to accommodate binary vector strings of larger sizes. Drawback of this adder is that the delay increases linearly with the bit length. Each full adder has to wait for the carry out of the previous stage to output steady-state result. The advantages of the RCA are lower power consumption as well as a compact layout giving smaller chip area.

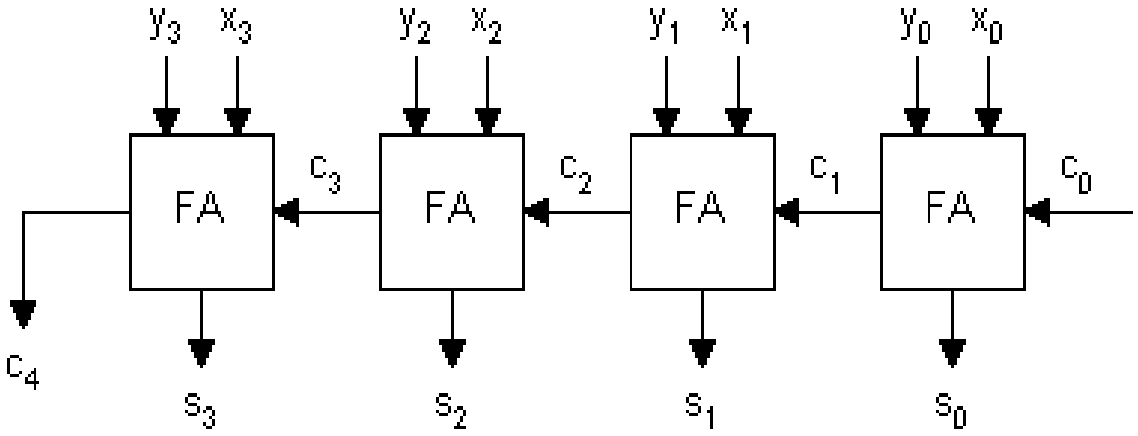

Fig 3:4-bit Ripple Carry Adder

Carry Look Ahead Adder

The carry look-ahead adder calculates the carry signals in advance, based on the input signals. The result is a reduced carry propagation time. The carry looks ahead structure consists of propagate /generate generator, sum generator and carry generator. The Boolean expressions for carry look ahead adder are,

$P_i = A_i \oplus B_i$ carry propagate
$G_i = A_i \ B_i$ carry generate
$S_i = P_i \oplus C_i$ sum
$C_{i+1} = G_i + P_i \ C$ carry out

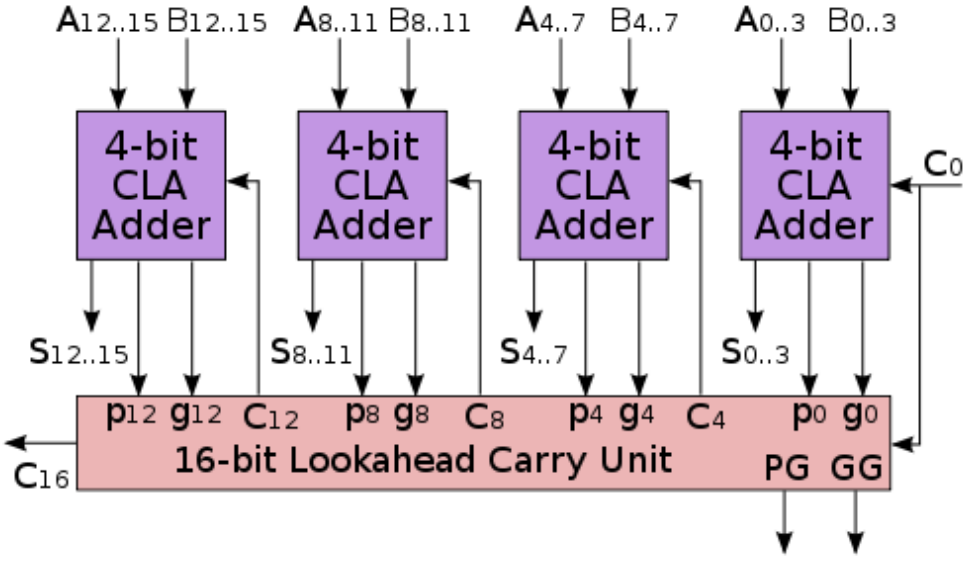

Fig 4: 16-bit Carry look ahead adder

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The Carry Look Ahead Adder is able to generate carries before the sum is produced using the propagate and generate logic to make addition much faster.

Carry Select Adder

The Carry Select Adder divides the number to be added into blocks and forms two sums for each block in parallel, one with a carry in of ZERO and the other with a carry in of ONE. Carry-select adder is to compute alternative results in parallel and subsequently selecting the correct result using a multiplexer, when the adder delivers the carry_in signal. Calculation of two sums is accomplished using two 4-bit ripple-carry adders. It enhances the speed performance and increases its area requirements.

Kogge-Stone Adder

The Kogge-Stone adder is a parallel prefix adder since it generates and propagates signals in advance. It is widely considered the fastest adder and it has high performance. Various blocks inside this adder are generate propagate block, gray cell, black cell and buffers [6].

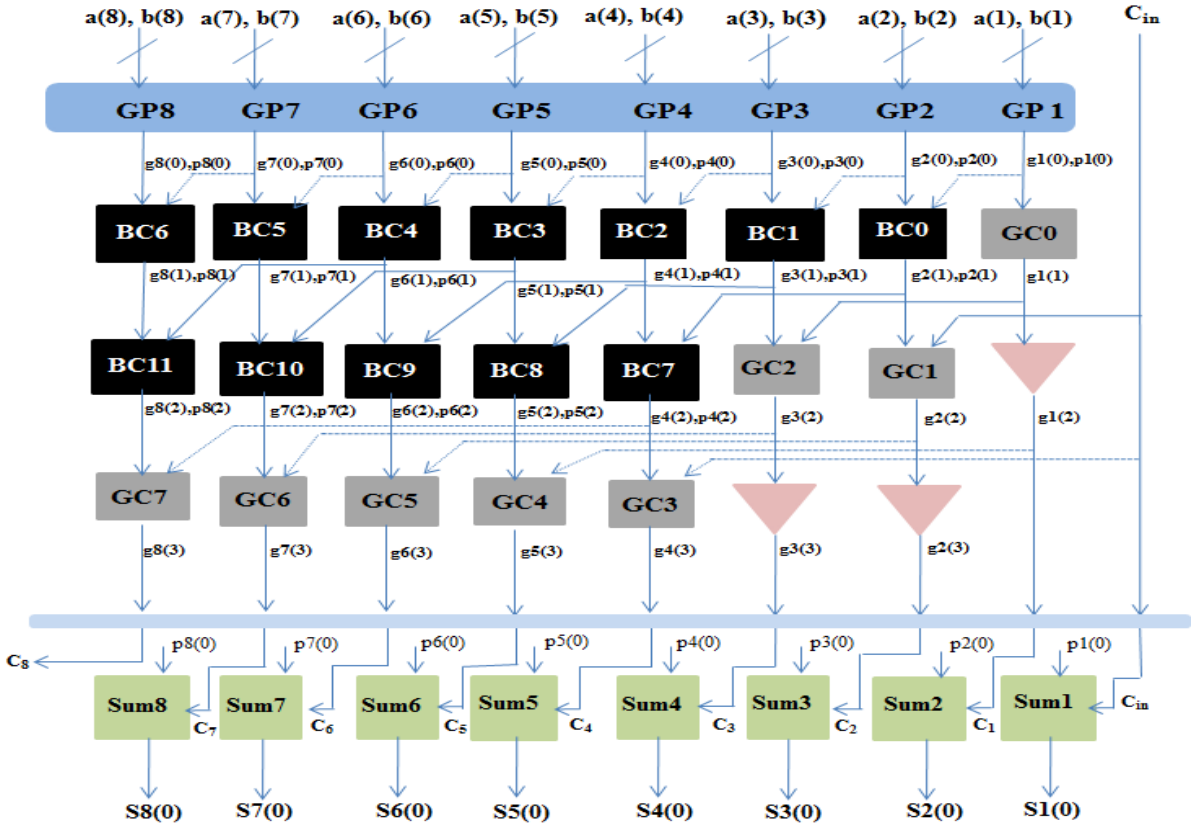

Fig 5: 8-bit Kogge-stone Adder

Sparse Kogge-Stone Adder

Sparse kogge-stone adder is nothing but the enhancements of the kogge-stone adder. The Sparse Kogge-Stone adder consists of several ripple carry adders on its lower half and a carry tree on its upper half. The number of carries generated is less in a Sparse Kogge-Stone adder compared to the regular Kogge-Stone adder. The functionality of the GP block, black cell and the gray cell remains exactly the same as in the Kogge-Stone adder. In this sparse kogge stone a reduction of number of stages is being done by reducing the generation and propagates units. The sparse kogge-stone adder has high fanout and less path delay [6].

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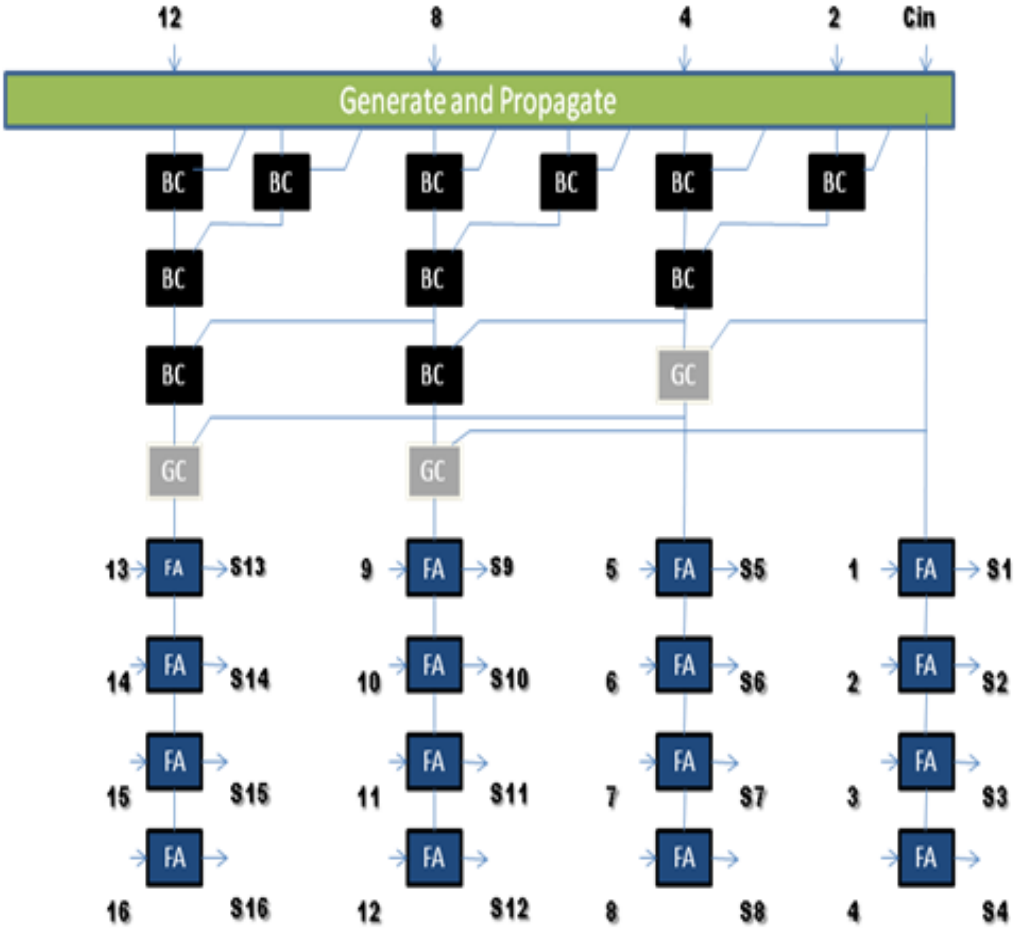

Fig 6: Sparse Kogge-Stone Adder

III. IMPLEMENTATION RESULT

The table II shows comparison of modified booth multiplier by use of various adders implemented using verilog. In comparison the Carry select adder has high occupied area and RCA takes less area. Kogge stone adder has maximum path delay compared to other adders and sparse kogge stone adder has lower path delay. As in the case of fan out the sparse kogge stone adder provides high fan out. It is much faster adder to add the partial product in multiplication process.

Performance Parameters	Ripple Carry Adder	Carry Look Ahead adder	Carry Select Adder	Kogge Stone Adder	Sparse Kogge Stone Adder
Occupied Slices	65	86	89	72	67
Path Delay (Max.)	20.955ns	20.947ns	21.558ns	22.779ns	20.581ns
Fan Out	4.74	4.46	4.30	4.74	5.17

Table II: Analysis of Modified Booth Multiplier

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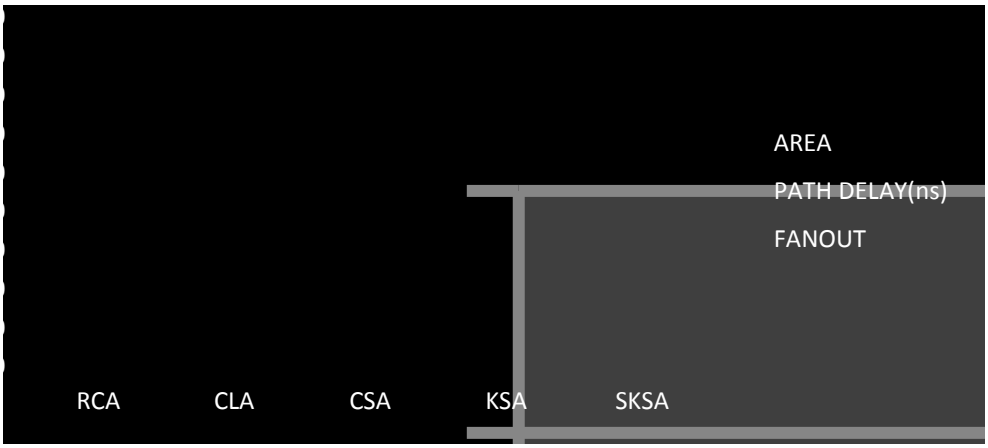

Fig 7: Comparison of adders in Modified Booth Multiplier

IV. CONCLUSION

In this Modified Booth Multiplier implemented by various adder technique. Partial product generated by booth encoder is added by various adders. RCA is occupied less area and Carry select adder has increased area. But path delay is increased in kogge stone adder and less in sparse kogge stone adder. Spare kogge stone adder is best amongst the all adders. It has less area, high fan out, less path delay, and it is the fastest adder. The number of carries generated is less in a sparse Kogge-Stone adder compared to the regular Kogge-Stone adder. So Sparse kogge stone adder is much faster to add the partial products.

V. FUTURE ENHANCEMENT

The Modified Booth algorithm has been implemented using hybrid adder to add the partial products in parallel for the final output. Hybrid adder is a combination of carry look ahead adder and carry select adder. It can be further extended by taking combination of any two adding techniques so that propagation delay is further reduced and enhances the speed of multiplication For higher inputs Radix 2^n multipliers will give better performance.

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