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Harmonic Analysis of Multilevel Inverter With Reduced Number of Switches and DC-Sources

K.Yogameenal, S.Baskar, S.Kalpana

***Abstract*— In this paper Harmonic analysis of new multilevel inverter cascaded topology was studied. In this proposed multi level inverter number of power semiconductor switches and dc sources was reduced. while comparing with the existing multi level inverter, the proposed inverter reduces harmonic content output in the inverter voltage and current.**

***Keywords*— cascaded multilevel inverter; distortion; harmonic; asymmetric module; sinusoidal pulse width modulation.**

I. INTRODUCTION

Multilevel inverters attained influential growth in almost every application chiefly due to its capacity in providing the output with extremely minimum distortions. They are also capable of absorbing the input voltage with minimum distortions. Multilevel inverters are preferred to conventional inverters because they are capable of generating step wave output which is similar to sinusoidal waves. Multilevel inverter reduces stresses along power semiconductor switches which results in reduction of EMC (electro magnetic compatibility) and it fasciliate in reduction of harmonic content in the system. Multilevel Inverters holds more advantages to that of the conventional inverter.

Multilevel inverters are trifurcated into three different branches such as diode clamped ,capacitor clamped and cascaded type multilevel inverter developed model utilizes cascaded multilevel inverter as they are capable providing desired output with minimum number of switches it is notable that when the number of switches is been reduced it totally reflects in reducing the stresses and complexity. Diode and capacitor clamped multilevel inverter holds more electro magnetic compatibility than cascaded type multilevel inverter. In Cascaded multi level inverter it holds separate H-Bridge series[15].in existing module it holds maximum number of switches in order to obtain the output of 31-level further it utilizes symmetric cascaded multilevel inverter topologies[1] .

In symmetric multilevel inverter it holds the dc source voltage of same magnitude .Where as in developed module it has minimum number if switches with symmetric cascaded multilevel inverter topology[10&11] .In symmetric multilevel inverter it has dc sources of different magnitude .its structure of levels are equal and capable of producing optimizing circuit layout. Developed module holds 12 switches with 4- dc sources. It is capable of producing 41-level output.

II. EXISTING MODEL OF 41 LEVEL MULTILEVEL INVERTER

The existing model has the detailed structural arrangement as shown in the fig1.circuit diagram represents the arrangement of existing multilevel inverter of 31-level.it composed of twelve subsystem with each subsystem holding four switches in it. Existing system is complex in nature. It holds more harmonic content especially due to its complexity. This induced to design a new harmonic less 41-level cascaded topology.

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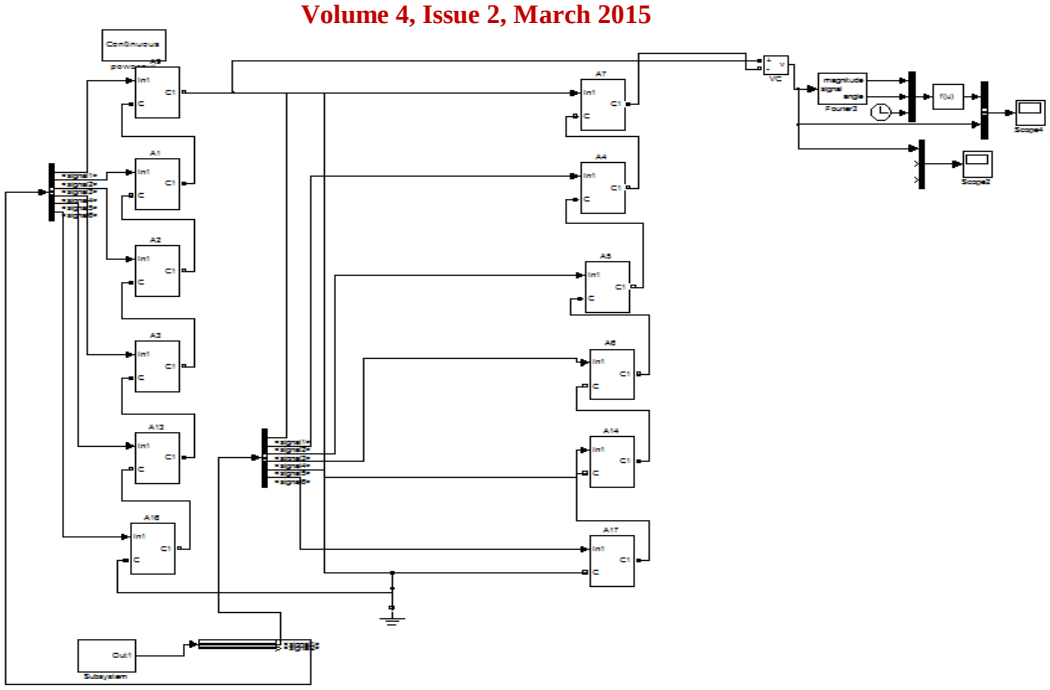

Fig 1. MATLAB Simulation of existing 41-level multilevel inverter

A. Working of Existing model

Existing model shown in the fig 2 comprises of totally 12 subsystem blocks each comprises of 4 switches in it. Totally, it comprises of 48 switches in order to generate 31 level multilevel outputs. It utilizes cascaded h-bridges topology in order to generate the required output.

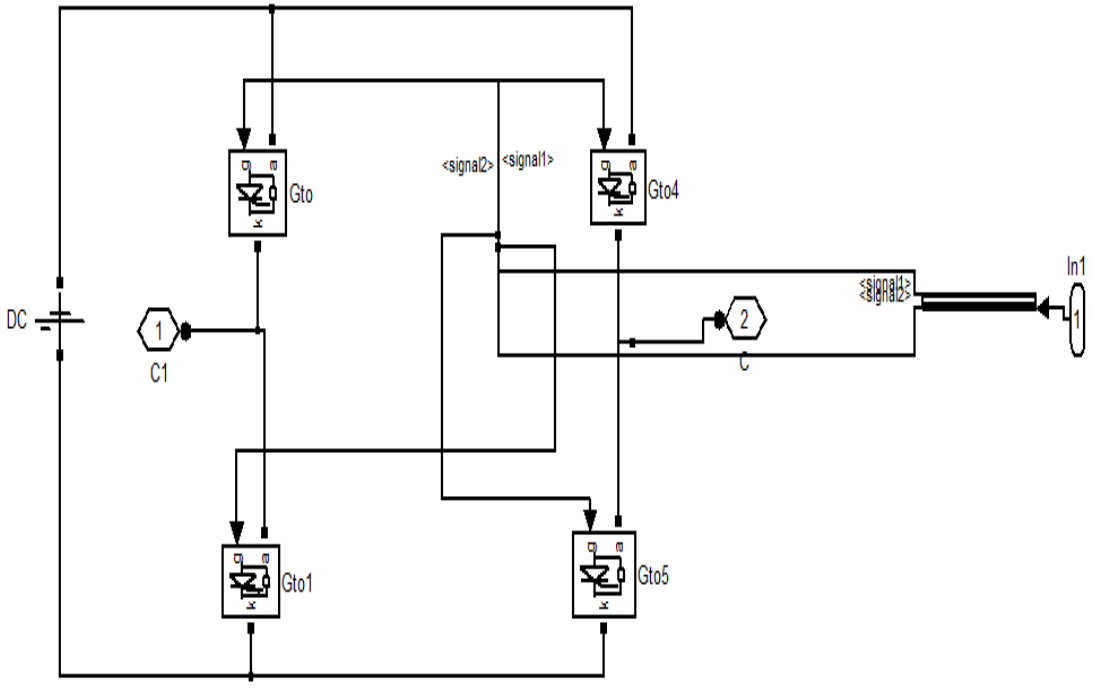

Fig 2. Individual subsystem of 41- level Existing multilevel inverter

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B. Output obtained from existing topology

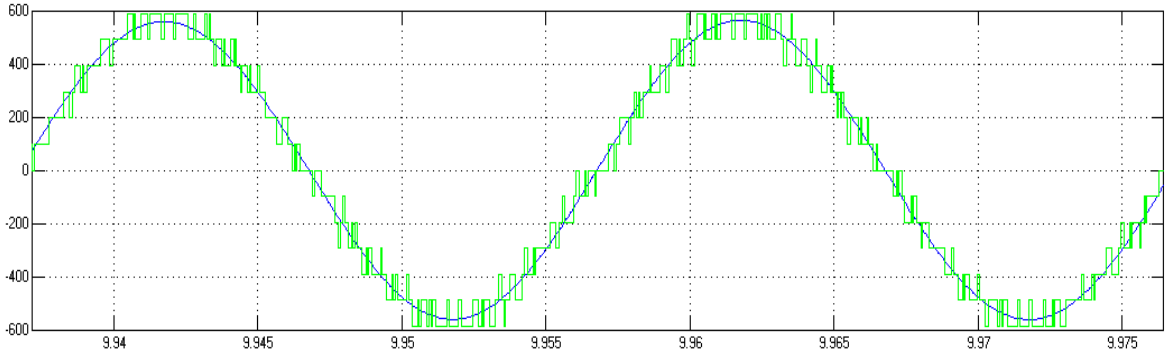

Fig 3. Output obtained from existing 41-level multilevel inverter

Output waveform of existing model comprised of 31-level output by using maximum number of 48 switches

C. FFT analysis of 41-level multilevel inverter

It is necessary to analyse the harmonic content found in the multilevel inverter of actual model, in order to find the differences in existing and proposed topologies. Though, existing model delivers actual required output. Its harmonic content is higher to that of proposed one and complexity in structure with stresses in switches is its other detriment. To overcome these detriment a new model is been proposed with the simple model capable of providing greater same output

III. PROPOSED MODEL OF 41-LEVEL MULTILEVEL INVERTER

The proposed model has the detailed structural arrangement as shown in the fig4.block diagram represents the arrangement of developed multilevel inverter of 41-level.it composed of pulse modulation block with switching arrangement connected series to that of the H-Bridge series then to the output. It uses minimum number of switches in order to provide stepped wave output of 40 levels. It comprises of the least number of switches and sources to deliver the expected output. Perfect cascaded arrangement with triggering switches at proper time phase helps in producing 40 level output. It is composed of 8 number of switches with separate H-Bridge connections which gives 12 no's switches. This work uses 12 switches with 4 Dc sources. Cascaded topologies model can be enhanced with two types to produce output [4]. Here asymmetric topologies have been used where the dc sources are not equal in magnitude. Switching is done in sequential manner in ordered to obtain perfect expected result.

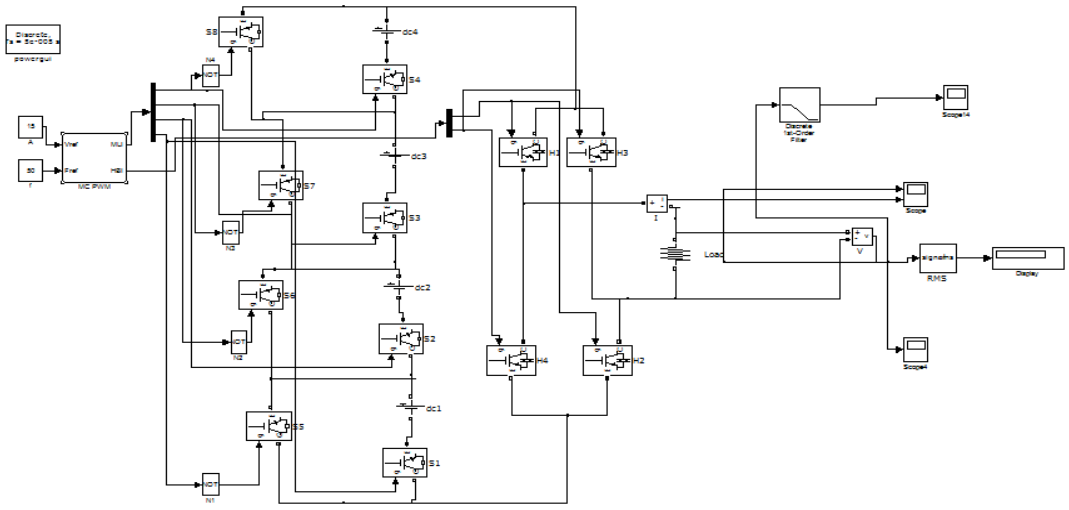

Fig 4. Proposed Model of 41-Level Multilevel Inverter

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IV. SWITCHING TOPOLOGIES

A. Switching topology of 41 level multilevel inverter

The developed topologies are unique and help in gradually reducing number of switches and sources. It utilizes of four asymmetrical DC level voltage sources for generating 41 levels dc voltage sources are been arranged in the fashion such as 2n, 3n, 4n…..Increments in the DC. Where n represent the lowest DC voltage source magnitude. All switches are adopting a unidirectional function in it. The figure 4 shows proposed topology. This figure has main eight switches in it. With additional H-bridges H1, H2, H3, H4 are used to form H-bridge components and it is been used to form both positive and negative sequence. When bridges H1 and H2 activate it forms the positive half cycle while H3 and H4 forms the negative half cycle of the system in order to generate output sequentially to provide stepped 41- level Proposed model comprises of 12 switches which comprises of eight main switches with four in each leg and the second series switches comprises of DC sources arrangement in between each switches. With sources having different amplitude in it. And it is been connected in series to that of H-bridge and delivered to load..Sinusoidal pulse width modulation is been implemented in order to obtain sequence of 41-level output. Number of switches implemented in it is 12 in number. 1 cycle holds harmonic content of 7.84 with increase in cycle level it is been gradually reduced to 5.83 ,5.37,5.20 and 5.12.this has been proved by comparing the FFT blocks of both actual and developed model and proved that actual has less THD and switches compared to that of the existing methodology.

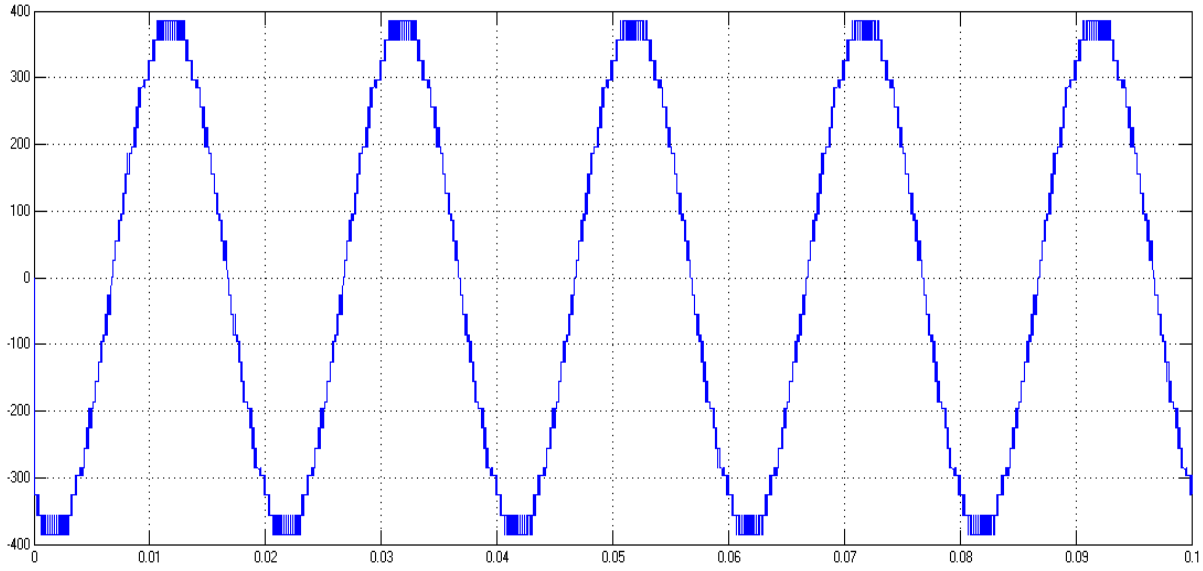

Fig 5 .Shows the Output of 41-Level Multilevel Inverter of Existing Model

V. SIMULATION RESULTS OF 41-LEVEL MULTILEVEL INVERTER

Proposed new simulation topology consist of circuits which is been authenticated through Simulink/MATLAB. 8 switches have been arranged in series with dc sources arranged.100V, 200V, 150V, 50V. Are the different magnitude level used in DC voltage sources [12]. Load resistance of 10 Ohm with Repeating sequence block is used to generate the switching pattern. Pulse generating units are used to trigger the H-bridge. Here FFT windows displays the total harmonic content been generated in the cycle and it is been portrait the different harmonic content been experienced .It is proved that harmonic content in the proposed one gradually reduces to that of the existing module. This makes the full fledged innovative technique with the generation of 41-level with reduced number of switches .thus the reduction of number of switches Reduces the switching stresses across switches it helps in reducing the complexity of the level. Further this also helps in increasing the life of the system. And its reduction of switches to that of the existing model with differences of 30 switches with minimum switches added advantage of this model.

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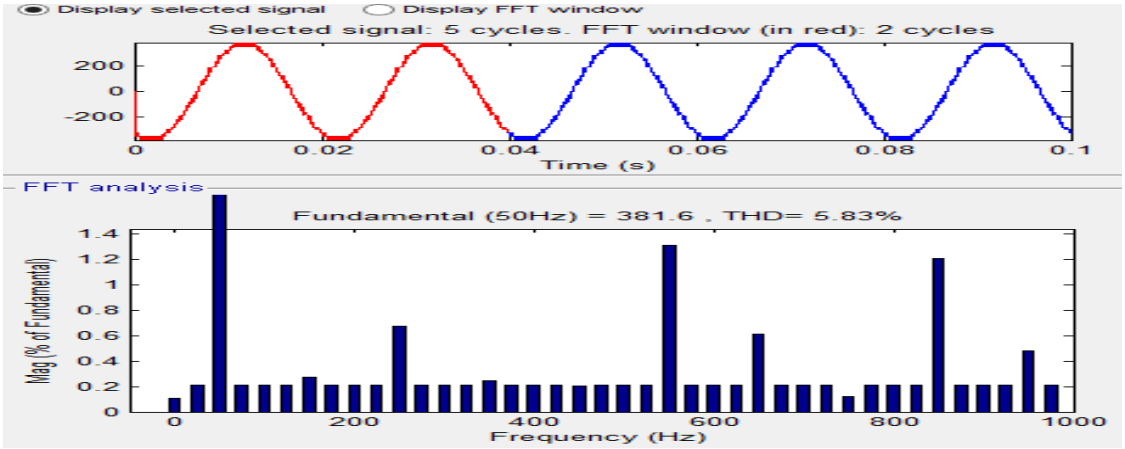

Fig 7. FFT for multilevel inverter of proposed model

These above attached FFT figures. Shows the FFT analysis denoting the reducing of harmonic content with increase in number of cycle

VI. COMPARISON OF EXISTING 31 LEVEL AND PROPOSED 41 LEVEL INVERTER

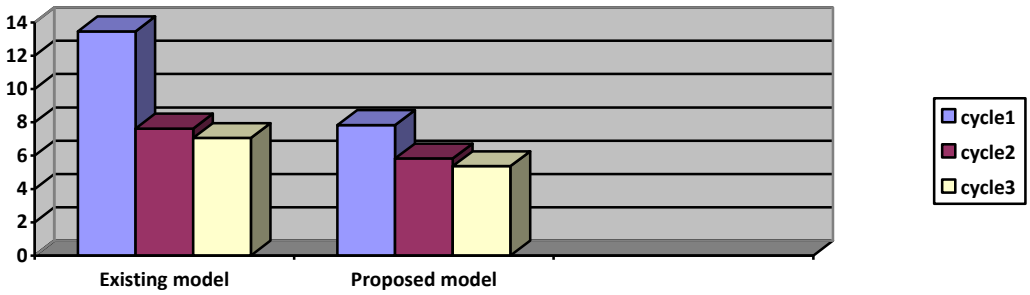

FIG 8: COMPARISON OF THD CONTENT OF EXISTING AND PROPOSED MODEL

Table 1: comparison of existing and proposed model

S.NO	Existing model	Proposed model
1	31 level output	41 level output
2	12-dc source	4-dc source
3	48 switches	12 switches

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VII. CONCLUSION

The performance of 41-level multilevel inverter using cascaded topology with reduced number of switches and dc sources are analysed. Results illustrates that output voltage and output current are at time of developed model is better while comparing with the existing topologies. The proposed Pulse width modulation Technique produces less Total harmonic distortion and improves power quality as per IEEE Standard of 5.19. This reduces the complexity and design of circuit. The proposed topology was implemented in Mat lab/Simulink software.

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