



ISSN: 2319-5967

ISO 9001:2008 Certified

International Journal of Engineering Science and Innovative Technology (IJESIT)

Volume 3, Issue 4, July 2014

# Low Power CMOS Flash ADC

C Mohan, T Ravisekhar

**Abstract**— The present investigation proposes an efficient low power encoding scheme intended for a flash analog to digital converter. The designing of a thermometer code to binary code is one of the challenging issues in the design of a high speed low power flash ADC. An encoder circuit translates the thermometer code into the intermediate gray code to reduce the effects of bubble errors. The implementation of the encoder through pseudo NMOS logic is presented. To maintain the high speed with low power dissipation, CMOS inverter has been used as a comparator and by adjusting the ratio of channel width and length, the switching threshold of the CMOS inverter is varied to detect the input analog signal. To maintain the high speed with low power dissipation, the implementation of the ADC through pseudo NMOS logic. The proposed ADC is designed using 90nm technology in 1.2 V power supply using HSPICE tool.

**Index terms:** Analog to digital converter, Flash ADC, Pseudo NMOS logic, Pseudo Dynamic CMOS logic multi threshold voltage CMOS inverters.

## I. INTRODUCTION

### A. Concept of ADC

The flash ADC is a fastest speed compared to other ADC architectures. Therefore, it is used for high-speed and very large bandwidth applications such as radar processing, digital oscilloscopes, and so on. The flash ADC is also known as the parallel ADC because of its parallel architecture. Figure 1 illustrates a typical flash ADC block diagram. As shown in Fig.1, these architecture needs  $2^n - 1$  comparators for a n-bit ADC; for example, a set of 7 comparators is used for 3-bit flash ADC. Each comparator has a reference voltage that is provided by an external reference source. These reference voltages are equally spaced by  $V_{LSB}$  from the largest reference voltage to the smallest reference voltage  $V_1$ . An analog input is connected to all comparators so that each comparator output is produced in one cycle. The digital output of the set of comparators is called the thermometer code and is being converted to gray code initially (for minimizing the bubble errors) and further changed into a binary code through the encoder [1]. However, the flash ADC needs a large number of comparators as the resolution increases. For instance, a 6-bit flash ADC needs 63 comparators, but 1023 comparators are needed for a 10-bit flash ADC. This exponentially increasing number of comparators requires a large die size and a large amount of power consumption [3]. The encoder is designed using pseudo NMOS logic style for achieving highest sampling frequency of 5GS/s and low power dissipation.

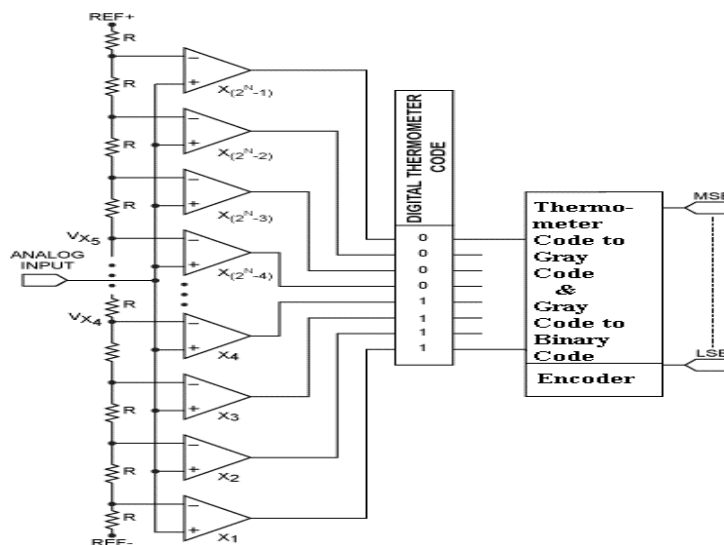


Fig 1: Flash ADC Block Diagram.



ISSN: 2319-5967

ISO 9001:2008 Certified

International Journal of Engineering Science and Innovative Technology (IJESIT)

Volume 3, Issue 4, July 2014

### B. Design of the Encoder

Conversion of the thermometer code output to binary code is one of the bottlenecks in high speed flash ADC design [2]. The bubble error usually results from timing differences between clock and signal lines and it is a situation where a '1' is found above zero in thermometer code. For very fast input signals, small timing difference can cause bubbles in the output code. Depending on the number of successive zeroes, the bubbles are characterized as of first, second and higher orders. To reduce the effect of bubbles in thermometer code, one of the widely used methods is to convert the thermometer code to gray code [5, 6]. The truth table corresponding to 2 bit gray code is presented in Table 1. The relationship between thermometer code, gray code and binary code is given below.

$$G2=T1$$

$$G1 = \text{not}(T2) T0$$

$$B0 = G2 \text{ XOR } G1$$

$$B1 = G2$$

The equations for this encoder are derived from the truth table provided in Table 1.

T2	T1	T0	G1	G0	B1	B0
0	0	0	0	0	0	0
0	0	1	0	1	0	1
0	1	1	1	1	1	0
1	1	1	1	0	1	1

Table 1. Gray Code Encoder Truth Table

### C. Implementation of Encoder

There are different logic styles to implement the encoder design. Generally the implementation will be do using static CMOS logic style. The advantage of static CMOS logic style is that it is having the lowest power consumption with a lower speed. So for achieving a low power with high speed, other logic styles are preferred. Here the design is implemented using logic style called pseudo NMOS logic [8]. The pseudo NMOS logic circuit consists of a PMOS transistor with gate connected to ground, a bunch of NMOS transistors for the implementation of the logic style in the pull down network and an inverter. For the implementation of a specific logic circuit with N inputs, pseudo NMOS logic requires N+1 transistors instead of 2N transistors in comparison with static CMOS logic. Pseudo NMOS logic is an attempt to reduce the number of transistors with extra power dissipation and reduced robustness.

The PMOS transistor in the pull up network is connected to ground that will make the pull up network to be pulled on all the time. The output will be evaluated conditionally depending upon the value of the inputs in the pull down network. The inverter on the output transforms the inverted gate to non inverted gate. Since the voltage swing on the output and the overall functionality of the gate depend on the ratio of the NMOS and PMOS sizes, the transistor sizing is crucial in the implementation design. The disadvantage with pseudo NMOS logic is that it has static power consumption. (The power dissipation occurs when a direct current flows between VDD and ground. That is when both pull up and pull down networks are switched on simultaneously). The nominal high output voltage of (VOH) of pseudo NMOS logic is VDD inverter is added at the output side. This will improve the noise margin of the circuit. In spite of static power dissipation, the pseudo NMOS logic



ISSN: 2319-5967

ISO 9001:2008 Certified

International Journal of Engineering Science and Innovative Technology (IJESIT)

Volume 3, Issue 4, July 2014

consumes less amount of power because of the reduced number of transistors and the absence of other components (resistors) used for the implementation in comparison with current mode logic. The transistor sizes are given in Table 2.

(W/L) PMOS	300nm/100nm
(W/L) NMOS	120nm/100nm

Table 2. Transistor Sizes

D. Simulation Results

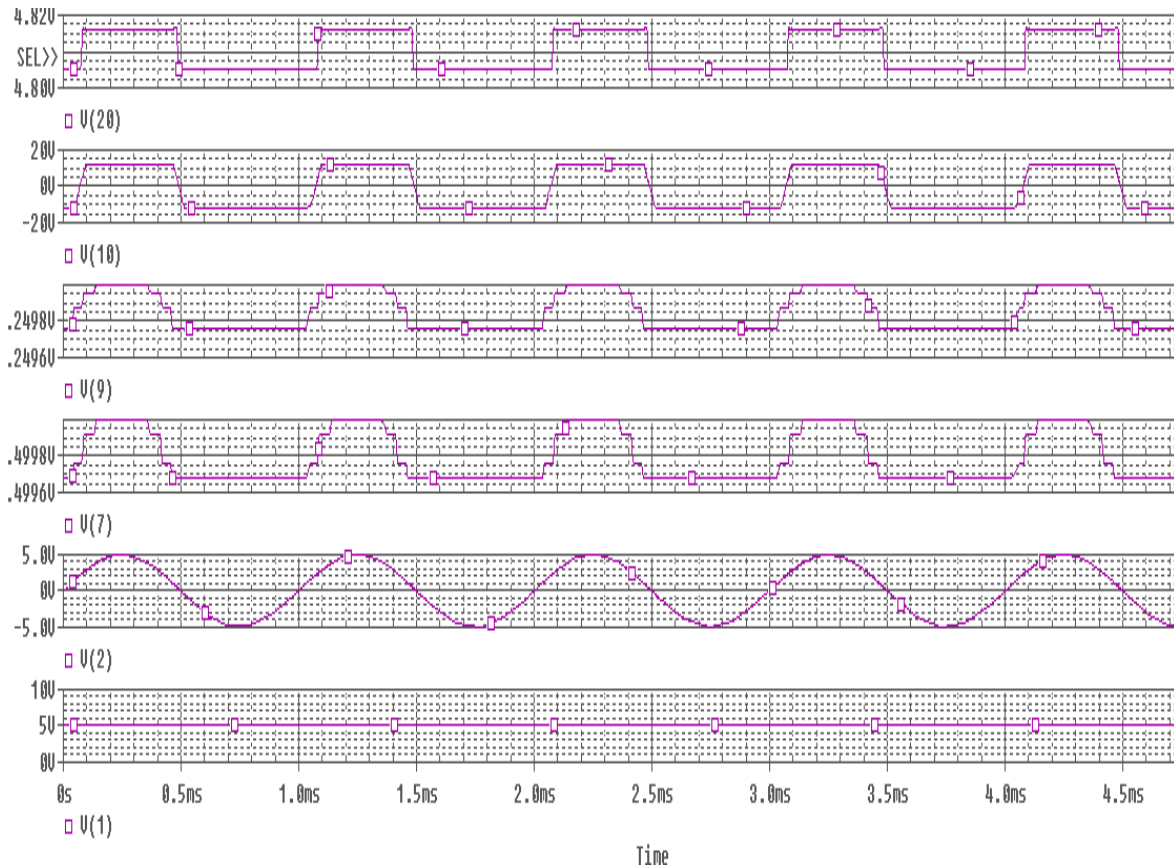


Fig 2: simulation results for General ADC.

II. MODIFIED FLASH ADC

A traditional n-bit flash ADC architecture uses 2n resistors and 2<sup>n</sup>-1 comparators to convert an analog signal to digital. This architecture has drawbacks like large input signal driving, high reference accuracy, high driving reference voltage and circuit complexity [10], [11]. CMOS inverters have been reported to be used in ADC designs [9]-[10]. In this work, this novel idea of employing CMOS inverters instead of analog comparators is considered for a flash ADC. CMOS is a combination of an n-MOSFET (NMOS) and a p-MOSFET (PMOS). CMOS inverter switching threshold (V<sub>th</sub>) is a point at which input is equal to output voltage (V<sub>in</sub>= V<sub>out</sub>) and in this region both PMOS and NMOS always operate in saturation region. If the input arrives at a particular threshold voltage, then the output state changes. V<sub>th</sub> can be obtained as [9]-[10]

$$V_{th} = V_{to} - V_{tp} + V_{tn} (k_n/k_p)^{1/2} / (1 + k_n/k_p)^{1/2} \dots\dots\dots 1$$



ISSN: 2319-5967

ISO 9001:2008 Certified

International Journal of Engineering Science and Innovative Technology (IJESIT)

Volume 3, Issue 4, July 2014

$$k_n = k'_n (w_n/w_p) \dots\dots\dots 2$$

$$k_p = k'_p (w_n/w_p) \dots\dots\dots 3$$

Where  $k'_n$  and  $k'_p$  are constant trans conductance parameters.  $V_{tn}$  and  $V_{tp}$  are the threshold voltage values of NMOS and PMOS respectively. As the voltages are constant,  $V_{th}$  depends on  $k_n$  and  $k_p$  values which decide the transition point of CMOS inverter [11]. If the ratio of  $k_n$  and  $k_p$  is decreased, the transitioned threshold voltage becomes high, otherwise, the transitioned inverter threshold voltage becomes low.  $k_n$  and  $k_p$  can be controlled by adjusting the width (W) and length (L) of NMOS and PMOS respectively. Based on this concept, various width/length ratios of CMOS inverters are designed to change their threshold voltages.

Each CMOS inverter thus has a specified threshold depending upon this ratio. The W/L ratios are define as  $Z_n=W_n/L_n$  and  $Z_p=W_p/L_p$ . By changing the ratio of  $Z_n$  and  $Z_p$ , we can obtain various transit threshold voltages of CMOS inverters to quantize the input level. All inputs of CMOS inverter are tied together to detect the analog input level. If the input arrives at a particular threshold voltage, then the output state changes. The basic architecture of the proposed flash ADC is shown in Figure 3. In a 4-bit ADC, 15 CMOS inverters are tied in parallel to detect the input signal level. The inverter output is array from MSB to LSB. For LSB bit, the  $Z_n/Z_p$  value should become small to increase the threshold voltage and for MSB bit, the  $Z_n/Z_p$  value should become large to decrease the threshold voltage.

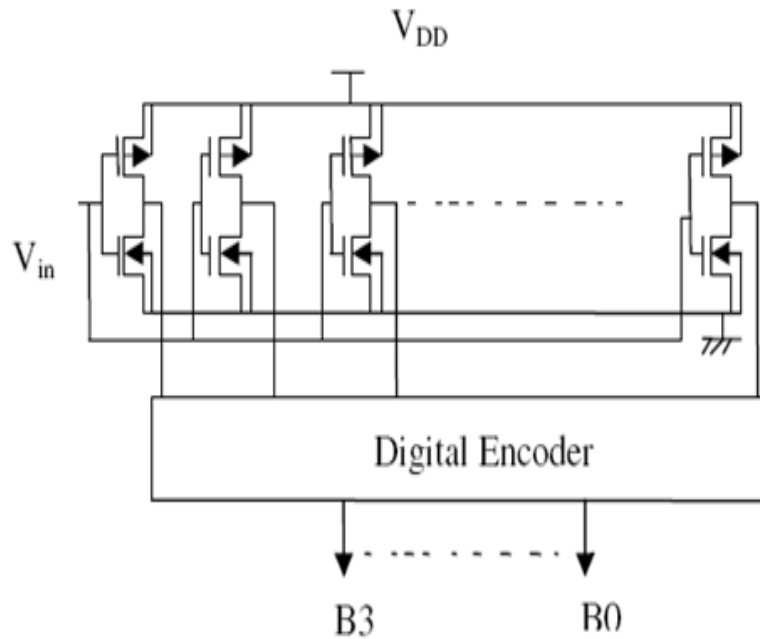


Fig 3.The architecture of proposed ADC.

Table 3. The transition point of 3 inverters in a flash ADC

Inverter	$Z_n/Z_p$	$V_{th}$ (V)
Inv1	330.00	2.75
Inv2	41.79	3.25
Inv3	13.20	5.50



ISSN: 2319-5967

ISO 9001:2008 Certified

International Journal of Engineering Science and Innovative Technology (IJESIT)

Volume 3, Issue 4, July 2014

III. SIMULATION RESULTS AND DISCUSSION

A. Simulation Results

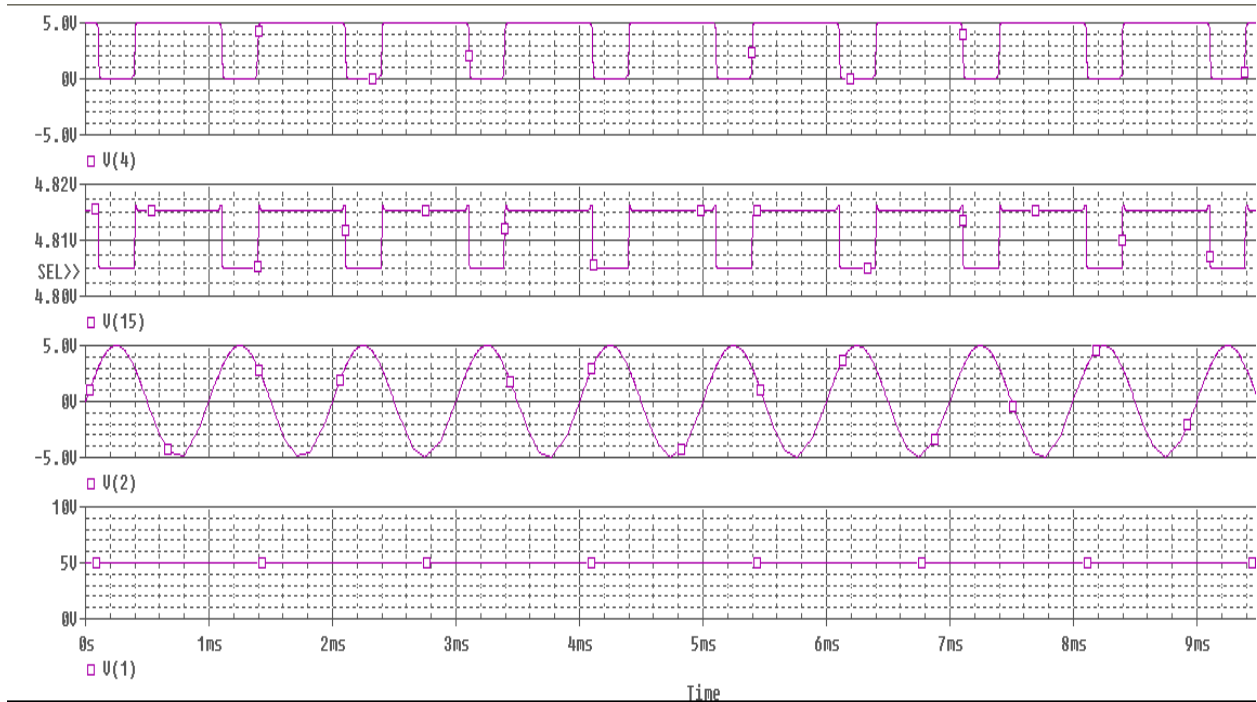


Fig 4: simulation results for modified flash ADC.

Results	Flash adc	Cmos flash adc
Architecture	Flash	Flash
Resolution	2 bits	2bits
Technology	Nano technology	Nano technology
Sampling frequency	1ghz	1ghz
Vdd	1.2v	1.2v
Power consumption	2.1053E2 watts	1.4316E-03 watts

The results show that the new design consumes less power than the traditional flash adc[2]. The power dissipation is reduced because of the usage of the reduced op-amps and resistors for the implementation of the logic. In comparison with the traditional flash adc, the proposed ADC is less cost.



ISSN: 2319-5967

ISO 9001:2008 Certified

International Journal of Engineering Science and Innovative Technology (IJESIT)

Volume 3, Issue 4, July 2014

#### IV. CONCLUSION

Low power architecture for a 2-bit CMOS inverter based flash ADC is presented using 90nm technology. The proposed ADC design can achieve very low power dissipation and compared with the traditional flash ADC, this proposed method can reduce power consumption as well as uses smaller silicon area. Hence the proposed ADC cost is reduced.

#### ACKNOWLEDGEMENT

The authors would like to thank Mr.T.Ravisekhar, Department of ECE for her valuable guidance.

#### REFERENCES

- [1] D.Lee, J.Yoo, K.Choi and J. Ghaznavi, "Fat-tree encoder design for ultrahigh speed flash analog to digital converters" I proc. IEEE Midwest Symp. Circuits Syst, pp 233-236, Aug 2002.
- [2] S. Sheikhaei, S. Mirabbasi, A. Ivanov, "An Encoder for a 5GS/s 4bit flash A/D converter in 0.18um CMOS", Canadian Conference on Electrical and Computer Engineering, pp 698-701, May 2005.
- [3] R.Baker, H.W.Li, and D.E. Boyce, CMOS Circuit Design, Layout and Simulation. Prentice Hall 2000.
- [4] Sunghyun Park, Yorgos Palaskas, Ashoke Ravi, Ralph.E.Bishop, and Michael P. Flynn, " A 3.5 GS/s 5-b Flash ADC in 90nm CMOS", IEEE Custom Integrated Circuits Conference 2006.
- [5] Niket Agrawal, Roy Paily, "An Improved ROM Architecture for Bubble error Suppression in High Speed Flash ADCs", Annual IEEE Conference, pp 1-5, 2005.
- [6] Mustafijur Rahman, K.L. Baishnab, F.A. Talukdar, "A Novel ROM Architecture for Reducing Bubble and Meta-stability Errors in High Speed Flash ADCs", 20th International Conference on Electronics, Communications and Computer, pp 15-19, 2010.
- [7] Vinayashree Hiremath, "Design of High Speed ADC", M.S. Thesis, Wright State University, 2010.
- [8] Jan M Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "Digital Integrated Circuits, a design perspective", second edition, Prentice Hall 2011.
- [9] S. Chang Hsia, Wen- Ching Lee, "A Very Low Power Flash A/D Converter Based on CMOS Inverter Circuit," IDEAS'05, pp. 107-110, July 2005.
- [10] A. Tangel and K. Choi, "CMOS Inverter as a comparator in ADC design," in Proc. ICEEE, 2001,pp. 1-5.
- [11] S. M. Kang and Y. Leblebici, CMOS Digital Integrated Circuits Analysis and Design, Tata McGraw-Hill Edition 2003.

#### AUTHOR BIOGRAPHY



**C. Mohan** received the B.Tech. Degree in 2011 in Electronics and Communication Engineering from VITT College of Engineering, Thanapalli. He is presently pursuing M.Tech in VLSI in Sree Vidyanikethan Engineering College (Autonomous), Tirupati and would graduate in the year 2014. His research interests include Digital Logic Design, VLSI and FPGA.



**T. Ravisekhar**, M.Tech., is currently working as an Assistant Professor in ECE Department of Sree Vidyanikethan Engineering College (Autonomous), Tirupati. He had completed M.Tech in VLSI Design, in Satyabhama University and received B.Tech from Sri Kalahasteeswara Institute of Technology, Srikalahasti. His research areas are Digital Design and VLSI Signal Processing.