ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 3, Issue 4, July 2014

Implementation of Five Level Buck Converter for High Voltage Application

Manu.N.R[1], V.Nattarasu[2]
[1] M.Tech in Industrial Electronics, SJCE, Mysore, [2]
Associate Professor, Dept. of ECE, SJCE, Mysore

Abstract- The buck converter topology with higher voltage in the HVDC distribution system is a major challenge in the power converter implementation. This paper presents a viability of non isolated five level buck converter for high voltage application and theoretical analysis for five level buck converter is carried out and discussed. The difficulty in implementation comes in the form of dv/dt loss across the switches. In order to check the performance, the experimental results for a prototype system of 750-V input voltage to 440-V output voltage, 8-KW power and frequency of 25 kHz are carried out. Mat lab based simulations are implemented.

Key words- Buck, Converter, Losses, Control, Ripple

I. INTRODUCTION

Multilevel converters have attracted interest in power conversion; they already are a very important alternative in high power applications. It has been shown that they are useful in virtually all power conversion processes such as ac-dc, dc-ac, dc-dc and ac-dc-ac.

The challenges and the opportunities associated with adopting the DC distribution scheme in the power systems, the issues like interaction between the power converters that are use to convert ac-dc and dc-ac and other challenging issue like proper grounding and neutral voltage shift are the major issues in the DC converter schemes[2].

Along with the increase in the capacity of offshore wind farms and the distance between the offshore wind farm and the land, the DC collection and the DC transmission grid, with the advantages such as reactive power and harmonics etc., becomes attractive under the growing trends of the offshore wind farm development. Recently, the HVDC technology is being attractive for the long distance power transmission of the large-scale offshore wind farm, which can effectively reduce the cable loss and cost [3-6].

The four switch full bridge dc to dc converter topology is basically for high input voltages, it gives one half of the input voltage across all the four switches, where in which the two legs of the converter are connected in series with each other across the input. Due to this the switching losses across switch reduces, where instead of each leg of the full bridge converter connected across DC input source [7]. And its application is limited to 10kV of input voltage.

The voltage stress on each of the switches in the multilevel converter is one third of the input voltage, and this can be obtained by soft switching method so that the switches are of low resistance and low voltage rating can be used [8-9].

And another common solution to reduce the voltage loss across switches are with series input and parallel output connections as mentioned in [10], and it is limited to the applications like low output and high input voltage. For high frequency operation the transformer isolated bidirectional dc to dc converter modules connected in input series and output parallel as stated above, where here the low voltage MOSFET switches are used, and its application is only for the medium voltage [10].

In order to achieve the high power, the high voltage and high current semiconductor switches are required. Currently the IGCT with breakdown voltage of (6.9kV) is the most commonly used semiconductor for high voltage application, and also the IGBT with breakdown voltage of (6.5kV) are used. So in practice for high switching frequency operation (>10 kHz) the most attractive switches are IGBT and MOSFET [11-12].

The semiconductor switches is with series connection is commonly found in the survey, the modularity is the main advantage of the above technique but the main disadvantage is the necessity of a complex balancing circuit [11].

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ISO 9001:2008 Certified
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Within these parameters, this paper presents a non isolated five level buck converter for high voltage application. The main features of this five level converter are: low harmonic distortion, low voltage stress across switches, low EMI noise, high efficiency, ability to operate without magnetic components.

Fig.1 shows the five level buck converter, which will be analyzed and discussed in this paper. The theoretical analysis, capacitor voltage active control as well as experimental results are shown in this paper.

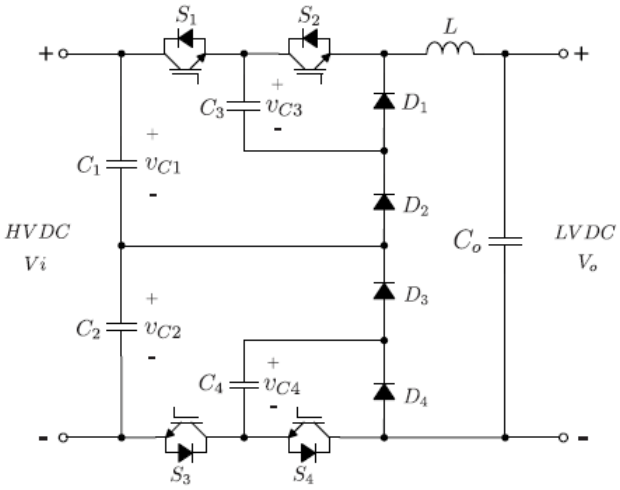

Fig. 1: Five level buck converter

The most critical components of the five level buck converter are the capacitors C1 and C2, because they are applied to the high voltage (i.e. half of the input voltage), and also all the high voltage converters use this feature [1] & [7].It may be necessary to change the number of capacitors connected in series in accordance with the input voltage of the converter. The voltage across the capacitors must be balanced for the safe operation of the proposed converter. The unbalanced voltage across the capacitors will make the switch voltages higher than the designed value. Thus, a capacitor voltage balancing active control is required in this converter. This issue is addressed in this work.

II. THEORETICAL ANALYSIS

The topology of the five level buck converter is taken from the flying capacitor multilevel inverters. Where they build the voltage levels by using the different levels of capacitors, the voltages of the capacitors add in each level resulting in increase in the voltage. But in the proposed converter it is the other way, it will decrease the voltage by the number of levels for each inclusion of the capacitor. Hence the topology acts as the buck converter. The theoretical analysis is performed considering the steady-state operation in continuous-conduction-mode of the five level Buck converter. The voltage over the semiconductors and the capacitors C3 and C4 is Vi/4, while the voltage across the capacitors C1 and C2 is Vi/2, where Vi is the input voltage. mentioned before, the capacitor voltages must be balanced for the correct operation of the proposed converter. So a modulation strategy is used to charge and discharge the capacitors in order to achieve voltage balancing. The five level buck converter is operated in four operating regions. The waveforms for each operating region are shown and explained. The expression for static gain, inductor current ripple and the capacitor voltage ripple are derived.

A. Modulation strategy and main wave forms

The modulation strategy adopted here is based on phase-shift PWM, with 90 degree phase shift between subsequent carriers. There are four carrier signals, and each carrier signal is used generate the gating pulse of one switch. And this technique allows the charge and discharge of each capacitor, and this implementation helps for active control of capacitor voltage balancing. This control is discussed in section 3. The five level converter operated in four operating regions, and it is shown in below Table 1.

Table 1: Operating region of five level buck converter

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Duty-Cycle	Output voltage limits	Operating regions
$d < ¼$	$0 - V_i/4$	R1
$¼ < d < ½$	$V_i/4 - V_i/2$	R2
$½ < d < ¾$	$V_i/2 - 3V_i/4$	R3
$¾ < d < 1$	$3V_i/4 - V_i$	R4

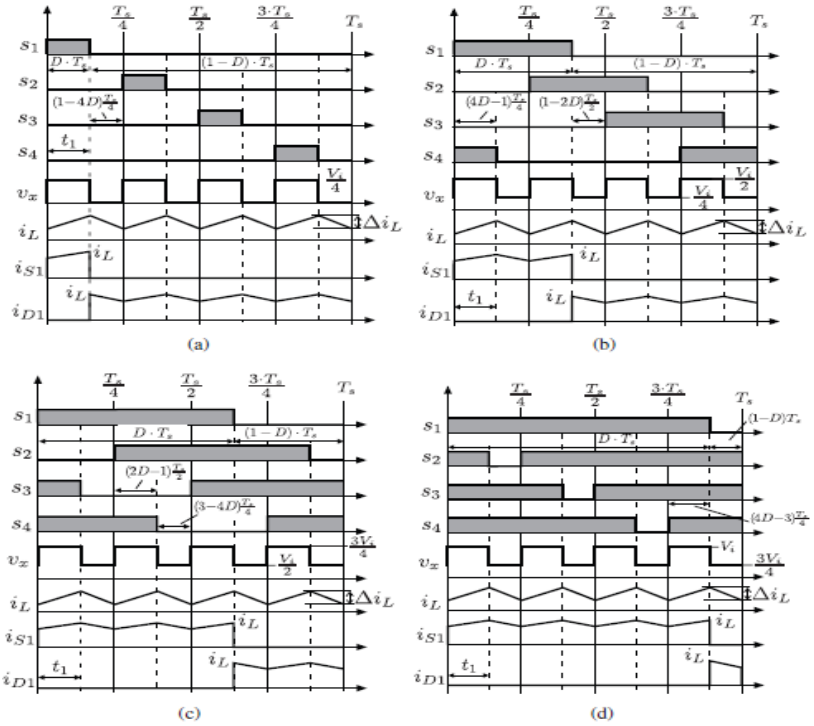

Fig. 2: Main waveform of five level buck converter

Fig. 2 shows the main wave forms (for the four operating regions) of the five level buck converter with switching period T_s. From the Fig.2 it is observed that the proposed converter presents 16 switching states. And in Fig. 2 v_x is the voltage before the low pass filter (LC section), and the average voltage across the inductor is given by equation (1) where the area under v_L (t) over the time period $T_s/4$ is considered.

$$\frac{4}{T_s}\int_{t_0}^{t_0+\frac{T_s}{4}} v_L(t)dt \qquad (1)$$

v_L (t) is the voltage across the inductor, that is $v_L(t) = v_x(t) - v_0(t)$.

B. Static Gain

The steady state operation requires that the inductor current at the end of the switching cycle be the same as that at the beginning, meaning that the net change in the inductor current over one period is zero. Where the one switching period is $0 - T_s/4$.

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$$\frac{4}{T_s}\int_{t_0}^{t_0+\frac{T_s}{4}} v_L(t)dt = 0 \quad (2)$$

By considering that the converter is operating in region R1,

$$\left(\frac{V_i}{4} - V_0\right) DT_s = V_0\left(\frac{1}{4} - D\right)T_s \quad (3)$$

By rearranging the equation (3) the mathematical expression of the static gain as a function of duty cycle D is obtained as shown in equation (4). And it shows that static gain of the five level buck converter is same as that of conventional buck converter.

$$D = \frac{V_o}{V_i} \quad (4)$$

C. Inductor Current Ripple

By considering the energy storing or the energy transfer state of the inductor, the current ripple in the inductor can be calculated and this expression is given in equation (5).

$$\Delta i_L = \frac{1}{L}\int_0^{t_1} v_L(t)dt \quad (5)$$

The time interval t_1 has different values depending on the operating region and it is obtained from Fig. 2.The current ripple through the inductor has different behaviour according to the operating region. So that equation (5) must be used for all operating regions of five level buck converter. Hence by changing the value of t_1 in all the operating regions we can get the current ripple equation for each operating region.

In region R1, $$\Delta i_L = \frac{1}{L}\int_0^{DT_s}\left(\frac{v_i}{4} - v_0\right)dt$$

And putting $(v_0 = Dv_i)$ and $(T_s = \frac{1}{f_s})$

$$\Delta i_L = \frac{V_i}{4f_sL}(1-4D)D, \quad D < \frac{1}{4} \quad (6.\text{ a})$$

In region R2, $$\Delta i_L = \frac{1}{L}\int_{T_s/4}^{DT_s}\left(\frac{v_i}{2} - v_0\right)dt$$

$$\Delta i_L = \frac{V_i}{4f_sL}\frac{(1-2D)(4D-1)}{2}, \quad \frac{1}{4} \le D < \frac{1}{2} \quad (6.\text{ b})$$

In region R3, $$\Delta i_L = \frac{1}{L}\int_{T_s/2}^{DT_s}\left(3\frac{v_i}{4} - v_0\right)dt$$

$$\Delta i_L = \frac{V_i}{4f_sL}\frac{(3-4D)(2D-1)}{2}, \quad \frac{1}{2} \le D < \frac{3}{4} \quad (6.\text{ c})$$

In region R4, $$\Delta i_L = \frac{1}{L}\int_{3T_s/4}^{DT_s}(v_i - v_0)dt$$

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$$\Delta i_L = \frac{V_i}{4f_s L}(1-D)(4D-3),\ \frac{3}{4} \le D < 1 \qquad (6.\ d)$$

The equations 6. (a) (b) (c) & (d) gives the inductor current ripple in all four operating regions, where f_s is the switching frequency.

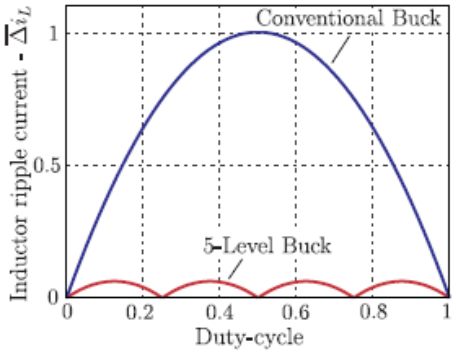

Fig. 3: Normalized inductor current ripple of the five level Buck and conventional Buck

Fig. 3 shows the normalized current ripple of the inductor for five level buck converter and the conventional buck converter. And the normalization is given by $\overline{\Delta}\, i_L = \Delta i_L 4f_s L/V_i$. The inductor current ripple in the fivel level buck converter reduces by 16 times. Further, from this the value of inductor can be given by equation (7).

$$L = \frac{V_i}{64.f_s.\Delta i_L} \qquad (7)$$

D. Capacitors Voltage Ripple

Here in this section the voltage ripple across the capacitors C1, C2, C3 and C4 are analyzed. Voltage ripple can be calculated by considering the energy storing state or the energy transfer state of the capacitor and is given by equation (8).

$$\Delta v_c = \frac{1}{C}\int_0^{\Delta t_c} i_C(t)dt \qquad (8)$$

Where Δt_c is the charge or discharge time interval and $i_C(t)$ is the instantaneous capacitor current. For the capacitor C1 and C2 the charge interval time is given by Δt_c, $\Delta t_C = DT_s$; for $D < 1/2$ and $\Delta t_C = (1-D)T_s$; for $D > 1/2$. And the charging current of these capacitors are $i_C(t) = I_L/2$. By substituting these values in equation(8) the voltage ripple across the capacitors C1 and C2 are obtained as shown in equation(9. a) & (9. b).

For capacitor $C_{1,2}$,

$$\Delta v_{c1,2} = \frac{1}{c_{1,2}}\int_0^{DT_s} \frac{I_L}{2}\, dt$$

$$\Delta v_{C1,2} = \frac{I_L}{2f_s C_{1,2}} D,\ D < \frac{1}{2} \qquad (9.\ a)$$

For capacitor $C_{1,2}$,

$$\Delta v_{c1,2} = \frac{1}{c_{1,2}}\int_0^{(1-D)T_s} \frac{I_L}{2}\, dt$$

$$\Delta v_{c1,2} = \frac{I_L}{2f_s C_{1,2}}(1-D),\ D > \frac{1}{2} \qquad (9.\ b)$$

And likewise for the capacitors C3 and C4 the charge interval time is given by, $\Delta t_C = DT_s$ for $D < 1/4$; $\Delta t_C = \frac{T_s}{4}$ for $1/4 < D < 3/4$; and $\Delta t_C = (1-D)T_s$; for $3/4 < D < 1$. The

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charging current of these capacitors are iC(t) =IL, And by substituting these values in equation(8) the voltage ripple across the capacitors C3 and C4 are obtained as shown in equation(10. a), (10. b) & (10. c).

For capacitor $C_{3,4}$,

$$\Delta v_{c3,4} = \frac{1}{c_{3,4}} \int_0^{DT_s} I_L \, dt$$

$$\Delta v_{C3,4} = \frac{I_L}{f_s C_{3,4}} D, \quad D < \frac{1}{2} \qquad (10.\ a)$$

For capacitor $C_{3,4}$,

$$\Delta v_{c3,4} = \frac{1}{c_{3,4}} \int_0^{T_s/4} I_L \, dt$$

$$\Delta v_{c3,4} = \frac{I_L}{4 f_s C_{3,4}}, \quad \frac{1}{4} < D < \frac{3}{4} \qquad (10.\ b)$$

For capacitor $C_{3,4}$,

$$\Delta v_{c3,4} = \frac{1}{c_{3,4}} \int_0^{(1-D)T_s} I_L \, dt$$

$$\Delta v_{c3,4} = \frac{I_L}{f_s C_{3,4}} (1 - D), \quad \frac{3}{4} < D < 1 \qquad (10.\ c)$$

The normalized voltage ripple of the capacitors with duty cycle is shown in Fig. 4. It is observed that the maximum voltage ripple occurs for D = 0.5 for all capacitors. Hence by assuming this maximum voltage ripple the capacitance expression can be derived as in equation(11).

$$C = \frac{I_L}{4 . f_s . \Delta C} \qquad (11)$$

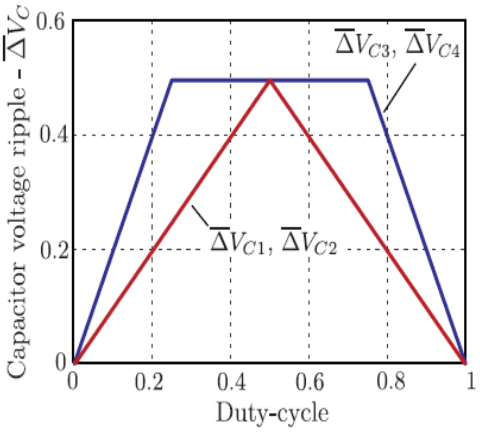

Fig. 4: Normalized voltage ripple of the capacitors Vs Duty cycle

III. CAPACITORS VOLTAGE BALANCING CONTROL

As mentioned before for the correct operation of the proposed converter, the capacitor voltages must be balanced. The following are some reasons for change in capacitor voltages: (1) voltage transient during the start up of the converter, (2) input voltage variations, (3) slight difference between the drive signals of the switches. The consequence of the unbalance in capacitor voltages result in increase in the voltage across the switches to unsafe values causing damages to the switches, which necessitates the need for a balancing strategy [13]. The

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converter uses flying capacitors for the proper sharing of a voltage between them, and the voltages are stabilized in a natural way by the load current and with the use of external passive RLC circuit [13]. The above balancing voltage active control can be extended to five level buck converter and which is analyzed in detail in this section. This analysis can be done by considering any operating region; however, the final results are the same.

Fig. 6 shows the modulator signal, all gating signals, carrier signals and capacitor currents. From this figure it is observed that perturbing the duty-cycle of the switch S1 (with a value of Δd1) affects the currents in the capacitors C1, C2 and C3. Consequently, the voltages of these capacitors also get affected. Likewise, perturbing the duty-cycle of switch S2 (with a value of Δd2) affects only the current of the capacitor C3. Perturbing the duty-cycle of the switch S3 (with a value of Δd3) affects the currents of the capacitors C1, C2 and C4. Perturbing the duty-cycle of the switch S4 (with a value of Δd4) affects only the current of the capacitor C4. Therefore from the above analysis it is concluded that it is possible to control the voltage of the capacitors C3 and C4 by perturbation in the duty-cycles of the switches S2 and S4 respectively. The voltages across the capacitors C_1 and C_2 cannot be controlled simultaneously (at a time), because the input voltage is constant and $V_i = V_{c1} + V_{c2}$. Thus only voltage across the capacitor C_1 or C_2 can controlled at a time. The parameter used to control the capacitor C1 voltage is Δd1. Here there are two possibilities for Δd2; one is Δd2 = 0 and the other is Δd2 = −Δd1. The second one is chosen in this paper. The effective duty-cycle of the switches is presented in Equation (12) and Fig.5 shows the block diagram of the modulator, considering the effective duty-cycle.

$$\begin{aligned} D_1 &= d + \Delta d_1 \\ D_2 &= d + \Delta d_2 \\ D_3 &= d - \Delta d_3 \\ D_4 &= d + \Delta d_4 \end{aligned} \tag{12}$$

It is very important to note that d is responsible for the output voltage and current, and Δd_k is responsible for the capacitor voltage balancing control.

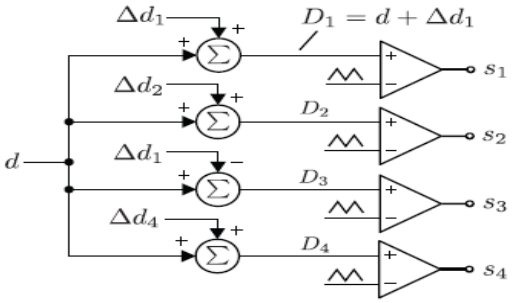

Fig. 5: Block diagram of the modulator

A. Capacitor Voltage Active Control

The Block diagram in Fig.7 shows the closed loop capacitor voltage active control system. Here the capacitors voltages are measured and then compared with the reference signal, resulting in the error signal. The error signal passes through the controller (proportional controller) and the duty-cycle perturbation is generated (Δd). At the same time the output voltage is measured and compared with the output reference voltage signal, resulting in error signal. The error signal passes through the controller (proportional controller) and the duty cycle (d) is generated. These Δd and d are added together before comparing with the carrier signals, and the outputs of these comparators are given to the switches as the gating signals to them.

IV. EXPERIMENTAL RESULTS

To verify the operation and evaluate the performance of the proposed five level Buck converter, an 8-kW prototype was designed and the proposed topology was experimentally verified. The converter specifications are

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ISO 9001:2008 Certified
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shown in Table 2. Due to the relation between the input and output voltage, the converter operates in the region R3.The selected components are shown in Table 3.

Table 2: Five level Buck converter Specification

Specification	Value
Input voltage	750- V
Output voltage	440- V
Output power	8- kW
Switching frequency	25- kHz
Inductor current ripple	1.8- A
Capacitor voltage ripple	4.4- V
Duty cycle	58.66

Table 3: Prototype Components

Parameters	Value
Output Inductor	260µH
Capacitors C1 to C4 and Co	41µF/1.3kV – film
Semiconductors	600V- IGBT

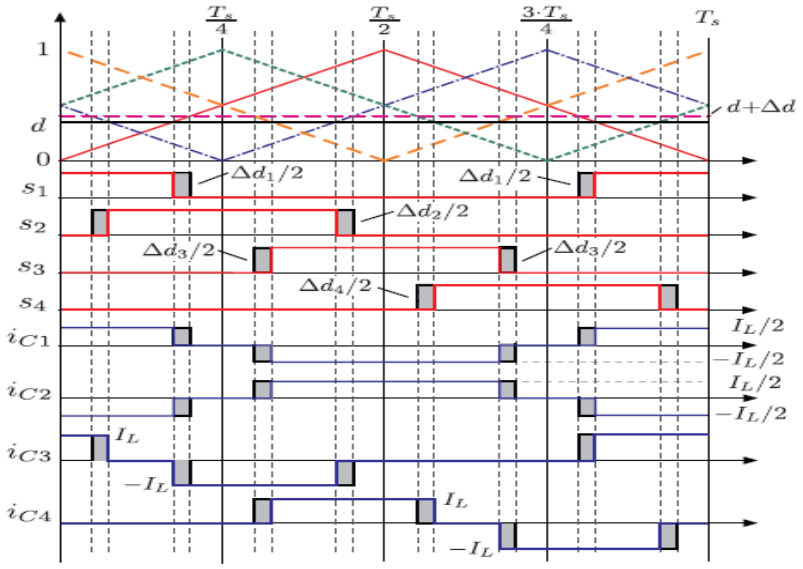

Fig. 6: Block diagram of the capacitor voltage control

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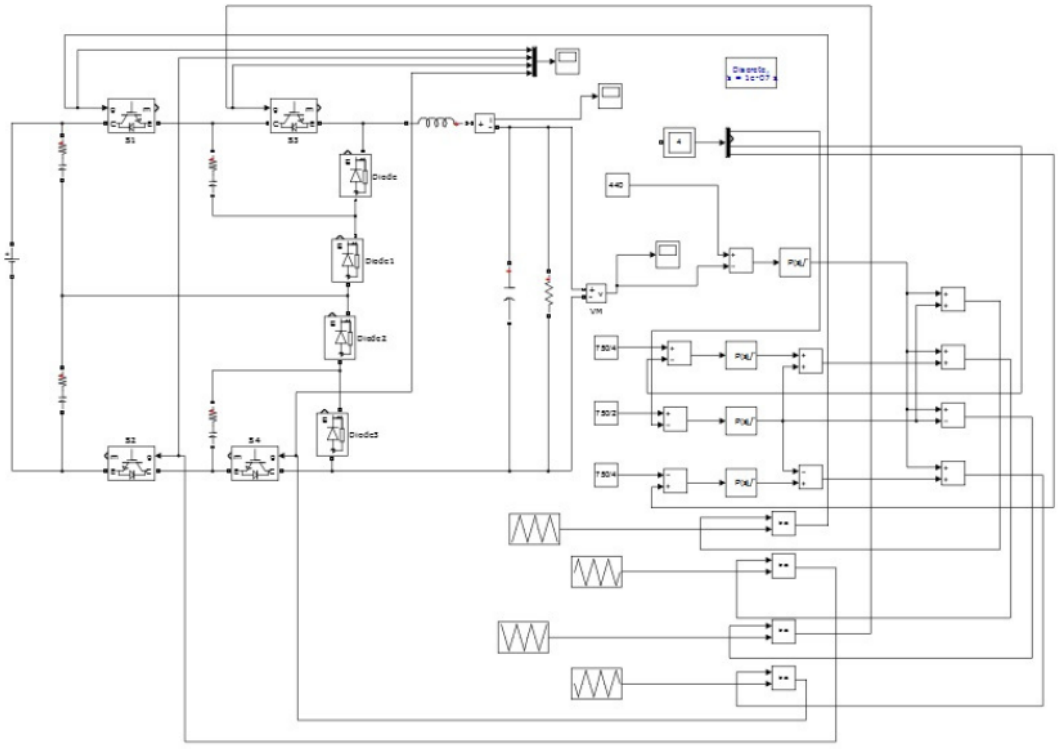

Fig.7: Block diagram of closed loop capacitor voltage active control system.

A. Steady-state operation waveforms

The steady state waveforms are shown in Fig. 8, Fig. 9, and Fig. 10. Fig.8 shows the output voltage (440V) of the proposed converter. Fig. 9 shows the Inductor or Output current (18A) of the proposed converter. And Fig. 10 shows the balanced voltages across capacitors under steady state. It may be observed that the voltage across each of capacitors C_1 and C_2 is close to 375V, while that across each of capacitors C_3 and C_4 is close to 187.5V.

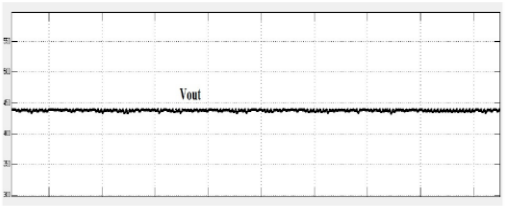

Fig.8: Output Voltage

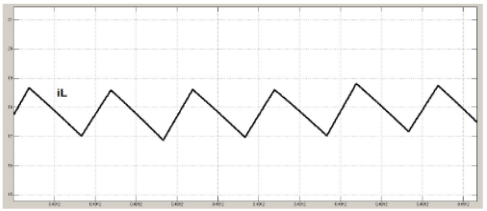

Fig. 9: Inductor Current

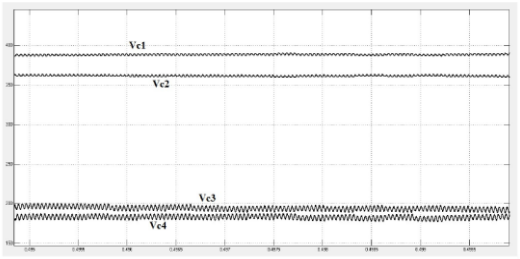

Fig.10: Capacitors voltages in steady state

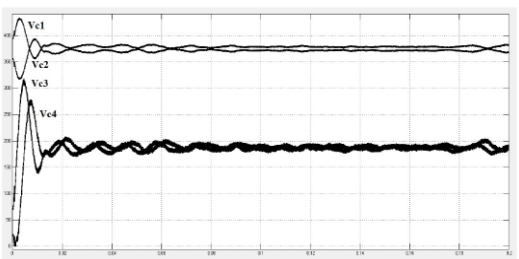

Fig.11: Capacitors voltages under unbalancing condition

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Fig. 11 shows the Capacitor voltages under unbalancing condition. Where here the capacitor voltage active balancing circuit is completely removed from the model, since the converter was forced to work in unbalancing condition. And at a specific time the voltage balancing control start to act, this we can observe in above Fig. 11.

V. CONCLUSION

A non isolated five level Buck converter for high voltage application was proposed and structure was analyzed in detail in this paper. The advantages of this converter are absence of a transformer, a reduced number of components, a reduced volume of output filter and low voltage across the semiconductors. A capacitor voltage balancing active control was presented and analyzed in detail. We used the proportional controller to control the capacitors voltage. And experimental results are satisfied and it obtained from an 8-kW prototype converter.

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