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CMC Based T-Statcom with Modified Selective Swapping

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Abstract-This paper deals with the design methods of Cascaded Multilevel Converter (CMC) based Transmission STATCOM (T-STATCOM) and development of star-connected, 11-level CMC. Number of H-Bridges in the CMC, AC voltage ratings, the number of paralleled CMC modules in the T-STATCOM system, optimum value of series filter reactors are discussed. In the CMC module, the AC voltages are approximated to sinusoidal waves by stair case modulation and by the use of an optimized series input filter reactor. The stair case modulation and equalization of DC link capacitor voltages is achieved according to Modified Selective Swapping (MSS) algorithm. MSS is applied for every 400µs period if needed to obtain a perfect equalization of DC link capacitor voltages at the expense of higher switching frequency and hence switching losses. The steady-state performances of each HB, the 11-level CMC, and the MSS algorithm are also given in this paper by using MATLAB/SIMULUNK. The result shows that the capacitor voltages are balanced, there is improvement in voltage profile and power factor of the system is improved. The 11-level output voltage is observed from MATLAB/SIMULINK.

Keywords: **Cascaded Multilevel Converter (CMC), Modified Selective Swapping (MSS), Transmission STATCOM.**

I. INTRODUCTION

The employing of turn-off-capability based power converters instead of the use of inductor or capacitor banks for VAr generation in concept of STATCOM was firstly disclosed by Gyugyi [1]. In view of reactive power operation, STATCOM is like Synchronous Condensers (SC) connected to the power grid which is in fact a synchronous generator operating at no load. By changing field current of the SC, the reactive power generated/absorbed is changed [2]. The major drawback is their relatively slow transient response against rapid load changes. STATCOM may give instant response to the rapidly changes of the power grid to their power converters. Unlike SVCs, their reactive power capability is independent of the supply voltage variations and by switching power converters appropriately.

In these practical STATCOM systems, various power semiconductors have been employed i.e., silicon-controlled rectifiers (conventional fast switching thyristors) [3], Gate Turn-off thyristors (GTO) [4], Insulated Gate Bipolar Transistors (IGBT) [5], and Integrated Gate Commutated Thyristors (IGCT) [6]. Two-level, six-pulse bridge converters with relatively high switching frequencies and relatively have low installed capacities. These are usually the characteristics of Distribution type STATCOM (D-STATCOM) systems [7].

However, for Transmission type STATCOM (T-STATCOM) systems the power semiconductors in their converter systems should be switched at lower frequencies. That is why in practical applications of T-STATCOM systems either multi-pulse converters based on two-level six-pulse bridge [2] or three-level Neutral Point Clamped (NPC) [7] converters or Multilevel Converter (MC) s are to be utilized. Cascaded Multilevel Converter (CMC) s, and Diode Clamped Multilevel Converter (DCMC)s [5] are generally employed in T-STATCOM applications. These systems are connected to the High Voltage (HV) or extra high voltage (EHV) buses of the transmission systems via coupling transformers.

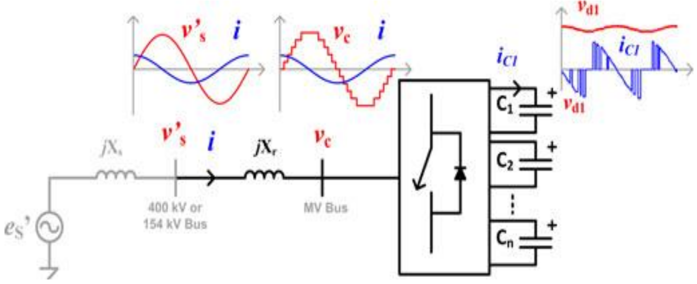


Fig. 1. Single-line diagram of a T-STATCOM based on a single CMC

This paper deals with the system design considerations and methodology for the power-stage design and implementation of an HV IGBT-based CMC for T-STATCOM applications. The Modified Selective Swapping (MSS) Algorithm is used to synthesize T-STATCOM voltage waveforms and to balance dc-link capacitor voltages perfectly.

The CMC presented in this paper has some advantages over the commercially available CMC and DCMC systems. These are as follows: 1) modularity and flexibility in the design permit higher CMC voltage ratings by increasing the number of HBs in each phase or by increase in the voltage rating of HV IGBTs in each HB; 2) operation without snubber; 3) no need of any auxiliary circuit for dc-link capacitor voltage balancing because of CMC and minimizes dc-link capacitance by the application of MSS algorithm; and 5) the CMC provides a rapid maintenance against failures owing to with drawable HB units. The steady-state performances of each HB, the 11-level CMC, and the MSS algorithm are also given in this paper by using MATLAB/SIMULUNK.

II. OPERATING PRINCIPLES

A. System Description

Fig. 1 shows the single-line diagram of a T-STATCOM based on a single CMC. It is shown to be connected to bus bar of the transmission system via a coupling transformer. Therefore, in Fig. 1, *Xr* represents the total leakage reactance of the coupling transformer and if needed the reactance of the series filter reactor. Waveforms of EHV or HV bus voltage *Vs'*, T-STATCOM line current *i*, CMC ac voltage *vc*, dc-link capacitor voltage *vd*1, and dc-link capacitor current i_{C1} are also sketched in Fig. 1. *e's* , *X's* , and *v's* denote, respectively, the internal source voltage, the source reactance, and EHV or HV bus voltage, all referred to the CMC side. The circuit diagram of a star-connected CMC consisting of *n* number of series-connected HBs in each phase is shown in Fig. 2.

The dc link of each HB in the CMC is equipped with a dc/dc converter controlled discharge resistor *R* to protect the dc-link capacitor *C* against dangerous over voltages and also to discharge *C* when the CMC is disconnected from the supply for inspection or maintenance purpose. *Lr* in Fig. 2 is the equivalent inductance of the total filter reactance *Xr* in Fig. 1. The three-phase voltage waveforms of the CMC are created by superimposing rectangular waves produced by n number of HBs. These voltage waveforms can be approximated to pure sine waves at supply frequency. Although line-to-neutral voltage waveforms have third harmonic voltage component and its integer multiples, these harmonics will not be present in the line-to-line voltage waveforms when the CMC performs balanced operation in the steady state.

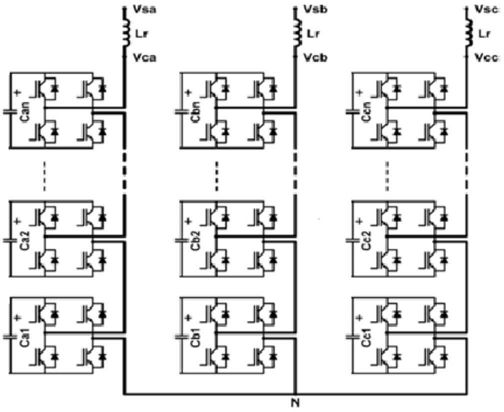


Fig. 2. Circuit diagram of a star-connected CMC consisting of *n* series connected HBs in each phase

A similar conclusion can be drawn also for the even harmonic voltage components. For a star-connected CMC, the line-to- neutral voltage waveforms has (s = 2n + 1) number of steps, the number of steps in line-to-line voltage waveforms (s = 4n + 1).

B. Reactive Power Control

The derivations of the active and reactive power expressions in the circuit in Fig. 1 are already given in [7]. Complex power input $S^{\rightarrow} = Ps + jQs$ to the T-STATCOM at EHV or HV bus is defined according to power sink convention. Active power Ps is always positive in the steady state. However, the sign of Qs depends upon the operation mode of the T-STATCOM, i.e., positive for the inductive operation mode and negative for the capacitive operation mode. The P in (1) compensates only for CMC losses.

$$P = \left(\frac{Vs'Vc}{Xr}\right)\delta \qquad (1)$$

Where δ is the phase angle of lead of $\vec{V}s'$with respect to $\vec{V}c$ and Vs' and Vc are the rms values of the fundamental components of vs' and vc , respectively. P is very small during the steady state operation of CMC and hence, δ takes a very low value (in practice, δ is around 1◦ [7]). Therefore, $\vec{V}s'$ and $\vec{V}c$ are nearly in the same phase.

When θ is defined as the phase angle of lag of $\vec{I}$ with respect to $\vec{V}c$, θ is nearly equal to+π2 for the inductive mode of operation in the steady state, while θ is nearly equal to -π2 for the capacitive mode. Therefore, reactive powers flowing on the supply side Qs and on the converter side Qc of the system in Fig.1 are approximately expressed by (2) and (3), respectively, as proven in [7].

TABLE I. Number of steps in CMC AC voltages for n number of HBs

Number of H-bridges, n	Number of steps in voltage	
	l-to-l s=4n+1	l-to-n s=2n+1
3	13	7
5	21	11
7	29	15

If θ is defined as the phase angle of lag of $\vec{I}$ with respect to $\vec{V}c$, for the inductive mode of operation θ is nearly equal to+π2 in the steady state, and nearly equal to -π2 for the capacitive mode. Therefore, reactive powers flowing on the supply side Qs and on the converter side Qc of the system in Fig.1 are approximately expressed by (2) and (3), respectively, as proven in [7].

$$Qs = Vs'[(Vs' - Vc)/Xr]$$

(2)

$$Qc = Vc[(Vs' - Vc)/Xr]$$

(3)

As can be understood from (2) and (3), in order to operate the T-STATCOM in the capacitive mode *Qs* should be made negative. This is achieved by making *Vc* greater than Vs'. The reverse is true for operation in the inductive mode. *Vc* will be adjusted to any desired value by varying the modulation index *M* of the CMC by a closed-loop control system.

III. DESIGN OF A CMC MODULE

In this paper, a three-phase, *Y* -connected, 11-level (Fig. 2) CMC module is designed. The ac voltage of the CMC is chosen to be *Vc* = 12 kV line-to- line and its constant dc-link voltage is *V*dc = 9500 V. Technical specifications of CMC and HB are given in Table II. This section describes the design of the HB circuit in the CMC Module.

A. Design of an HBridge

To synthesize 11-level line-to-neutral voltage in Fig. 3 by using five HBs in each phase of the CMC, at any time each HB circuit should be operated in one of the following modes: 1) charging (CH); 2) discharging (DCH); and 3) by-pass (BYP). All possible operation modes of each HB are marked in Fig. 3 by CH1, CH2, DCH1, DCH2, BYP1, BYP2, BYP3, and BYP4.

The operation mode of any HB in the CMC at any time and the duration of this mode are determined by the dc-link equalization method (MSS with Δts = 400 μs). Furthermore, *M* dictates how many of five HBs are to be operated in the by-pass mode at any time. As an example, in order to create +3*Vd* voltage level in line-to-neutral voltage waveform, three HBs should be operated in the discharging or charging mode while the others should be operated in the by-pass mode. On the other hand, which HBs are to be operated in the charging or discharging mode is dictated by the equalization algorithm of dc-link capacitor voltages.

For each step of the 11-level line-to-neutral voltage waveform, operation modes for all HBs and the number of HBs in each mode are also marked in Fig. 3. In order to avoid complexity in the explanations, the theoretical line-to-neutral voltage waveform and associated table are prepared for the CSS method. However, in this study the MSS method has been applied to prototype CMC in order to obtain a better equalization of dc-link capacitor voltages. Therefore, on $\pm Vd$, $\pm 2Vd$, $\pm 3Vd$, and $\pm 4Vd$ voltage levels, two switching's from one HB to another HB on the average may take place according to the MSS algorithm with $\Delta ts = 400\ \mu$s. In other words, at each swapping, the operation mode of one HB is changed from the charging or discharging mode to the by-pass mode while the operation mode of another HB is changed from the by-pass mode to the charging or discharging mode. Voltage spikes arising from the application of MSS method and superimposed on 11-level line-to-neutral voltage waveforms do not lead to an operational problem for the T-STATCOM and power system because they are successfully suppressed by the total series reactance.

TABLE II. Technical Specifications of CMC and HB

Cascaded Multilevel Converters(CMC)	
Rated power	±12MVar
Rated voltage	12KV
Number of H-bridges per phase	5
Number of levels in voltage	Line-neutral—11 Line-to-line—21
Cooling system(Sweed water)	De-ionized water cooling
H-bridges(HB's)	
Rated power	±8KVar
Rated voltage	1.8KV rms
Power semi conductor	3300v, 1200A HV IGBT with parallel inverse diode
Effective switching frequency	500HZ
Design value of Dc linkvoltage	1900V dc
DClink capacitor	9.2mF(4.6mF//4.6mF) ±10%
	260A rms, 2000V dc
	250V peak-peak ripple

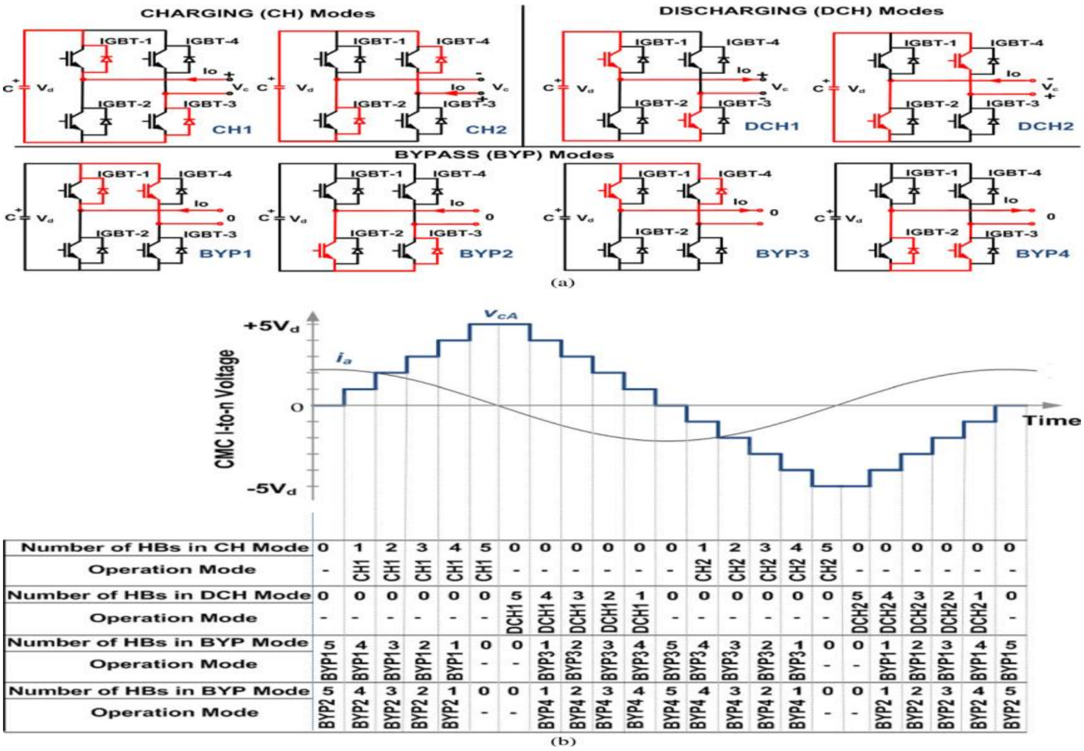
B. Choice of a DC-Link Capacitor

For the chosen HV IGBT modules, the dc-link voltage of each HB was taken to be 1900 VDC. It is kept constant in the steady state over the entire operating range of the T-STATCOM by controlling the active power flow from the supply and also by the dc-link capacitor voltage equalization method applied to the CMC. In the prototype T-STATCOM, ΔVd does not exceed ±12.5 V because of the successful performance of the MSS method applied. In view of the maximum allowable ripple content, 10% as a rule of thumb, the total dc-link capacitance of each HB is chosen to be 9.2 mF in Fig. 3. Field test results show that δVd does not exceed by 9% (170 V) over the entire operating range of the T-STATCOM, thus showing the success of the choice of the dc-link capacitance [10].

C. Modified Selective Swapping (MSS)

In the Modified Selective Swapping (MSS) algorithm, selective swappings are applied not only at level changes but continuously at a pre specified frequency during the operation of the CMC. Fig. 4 illustrates the application of the MSS method proposed in the paper. The only difference of MSS with Conventional Selective Swapping (CSS) is the application of swappings for a specified time not only the level changes but also during the levels. The flowchart of MSS method proposed in the thesis is given in Fig. 5.

The equalization algorithm uses these redundancy modes for DC link voltage equalization by inspecting the instantaneous DC link capacitor voltages. The individual capacitor voltages are firstly measured in each phase, and then sorted with respect to their instantaneous values. The use of the redundancy modes of HBs at each level change is determined by the charging or discharging states of the HBs which are defined as follows:



Number of HBs in CH Mode	0	1	2	3	4	5	0	0	0	0	0	0	1	2	3	4	5	0	0	0	0	0	0
Operation Mode	-	CH1	CH1	CH1	CH1	CH1	-	-	-	-	-	-	CH2	CH2	CH2	CH2	CH2	-	-	-	-	-	-
Number of HBs in DCH Mode	0	0	0	0	0	0	5	4	3	2	1	0	0	0	0	0	0	5	4	3	2	1	0
Operation Mode	-	-	-	-	-	-	DCH1	DCH1	DCH1	DCH1	DCH1	-	-	-	-	-	-	DCH2	DCH2	DCH2	DCH2	DCH2	-
Number of HBs in BYP Mode	5	4	3	2	1	0	0	1	2	3	4	5	4	3	2	1	0	0	1	2	3	4	5
Operation Mode	BYP1	BYP1	BYP1	BYP1	BYP1	-	-	BYP3	BYP3	BYP3	BYP3	BYP3	BYP3	BYP3	BYP3	BYP3	-	-	BYP1	BYP1	BYP1	BYP1	BYP1
Number of HBs in BYP Mode	5	4	3	2	1	0	0	1	2	3	4	5	4	3	2	1	0	0	1	2	3	4	5
Operation Mode	BYP2	BYP2	BYP2	BYP2	BYP2	-	-	BYP4	BYP4	BYP4	BYP4	BYP4	BYP4	BYP4	BYP4	BYP4	-	-	BYP2	BYP2	BYP2	BYP2	BYP2

Fig. 3. Eleven-level line-to-neutral voltage waveform and definition and sequence of HB operation modes (a) modes of CMC module (b) Waveform synthesizing

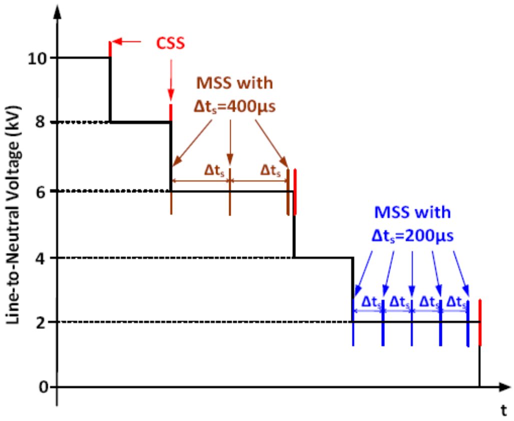


Fig 4 The illustration of CSS and MSS

If the current and the voltage both are positive or negative, the input power to the HB converter is positive and hence the DC link capacitor associated is going to be charged. On the other hand, if one of these quantities is positive while the other is negative, the power input to HB is negative and hence the associated DC link capacitor is going to be discharged. Therefore, in order to determine which HB's are going to be operated at each level, change the values of individual DC link capacitor voltages, polarity of the HB output voltage and direction of the line current should be measured. After determining the new status of DC link capacitors (charging or discharging) by this way, for charging HBs having the lowest DC link voltages will be put into operation and HBs having the highest DC link voltages, for discharging mode of operations.

IV. SIMULATION OF CMC BASED T-STATCOM

In this paper, a 154 kV, ±50 MVAr, H-Bridge (HB) based Multilevel T-STATCOM composed of five 12 kV, ±12 MVAr Cascaded Multilevel Converter (CMC) has been implemented primarily for the purposes of reactive power compensation and terminal voltage regulation, and secondarily for power system stability. Fig 6 shows the MATLAB model of the implemented 154 kV, ±50 MVAr T-STATCOM system. Five 12 kV, ±12 MVAr Cascaded Multilevel Converter (CMC) modules are connected in parallel via air-core reactors.

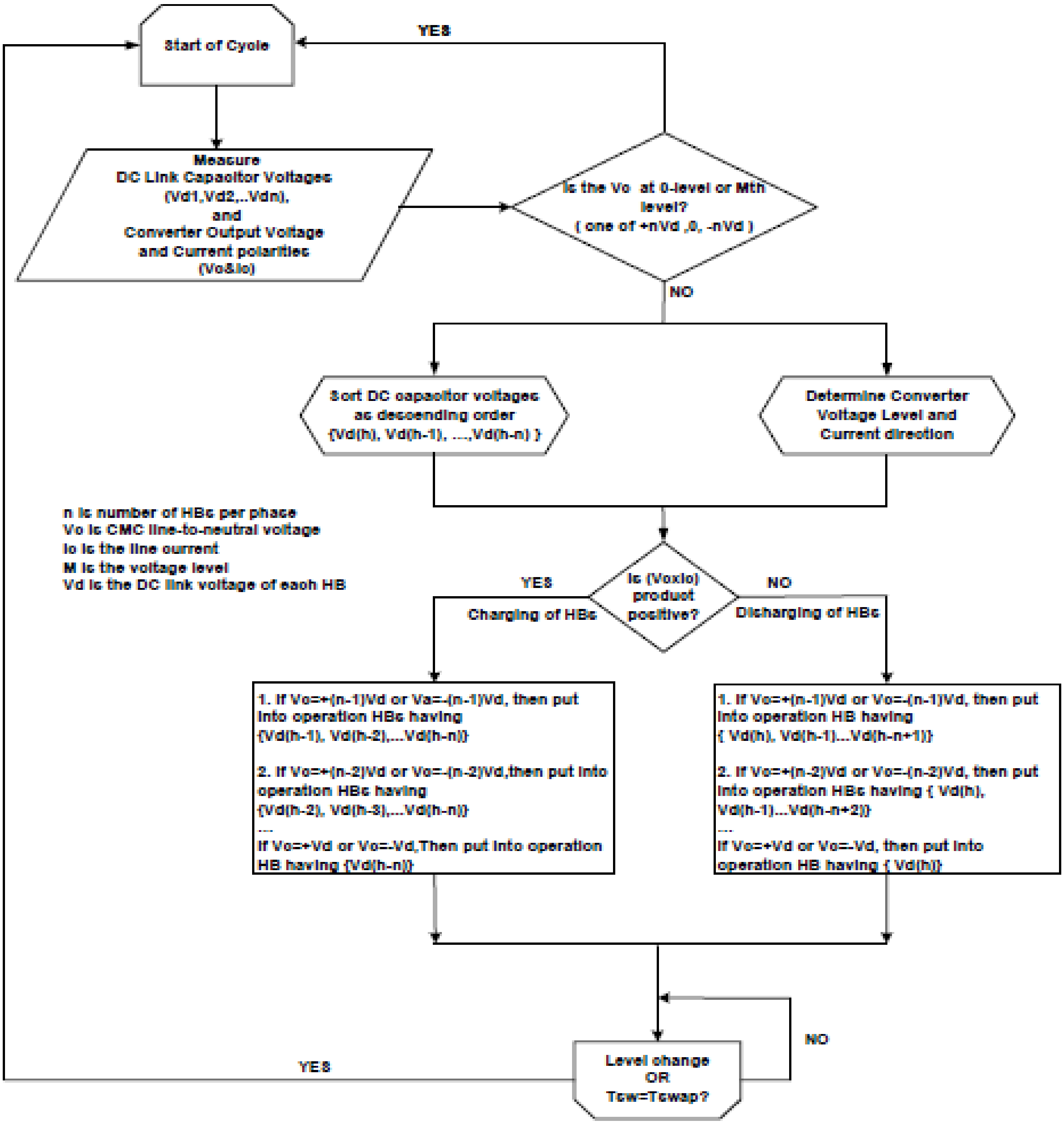


Fig. 5 The flowchart for MSS method employed in M-level CMC

The combination of these five CMC modules is then connected to 154 kV bus via coupling transformer. The ratings of the STATCOM converter used is shown in the table III. The STATCOM designed with those ratings is connected in parallel with the transmission line and the reactive power required is injected into the line. The range of reactive power compensated depends on the capacitor value.

To compensate the reactive power required in the line STATCOM is inserted in parallel with the line. The specifications of STATCOM is given in Table III. This is connected through a series inductance of 2.75mH. This STATCOM will have 2n+1 number of levels in its line-neutral voltage and 4n+1 levels in line-line voltage.

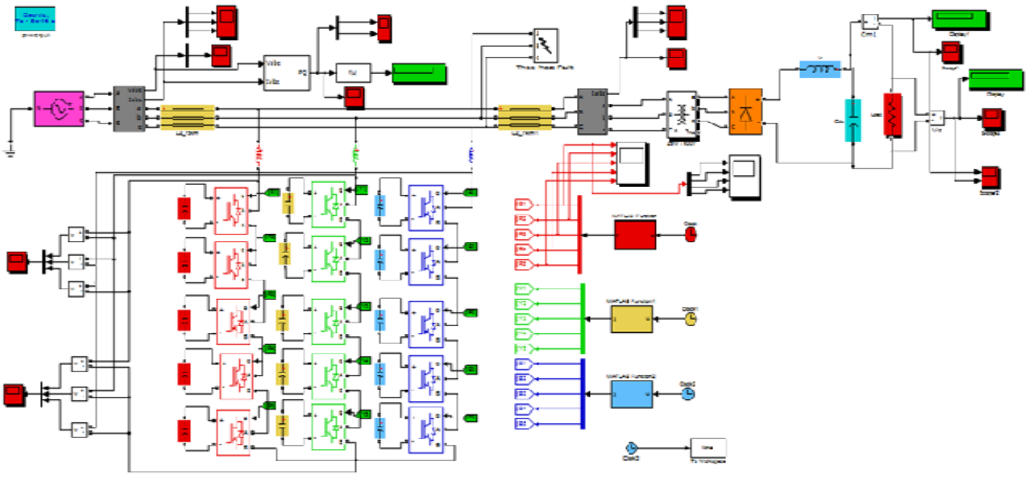


Fig. 6 MATLAB/SIMULINK model of the transmission system with CMC based T-STATCOM

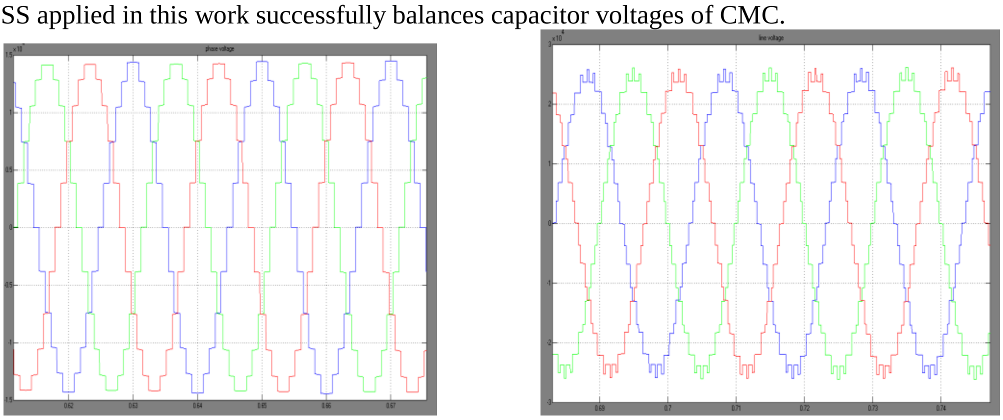
Table III. Specifications of T-STATCOM

T-STATCOM	
Rated voltage	154KV
Rated power	±50 Mvar
Number of CMC modules in parallel	5

V. SIMULATION RESULTS

The 11-level line-neutral voltage and 21-level line –line voltages are obtained by using MSS algorithm as shown in Fig 7. The MSS applied to the CMC causes generation of voltage spikes superimposed on both eleven-level line-to-neutral and 21-level line-to-line voltage waveforms. Power factor, load voltage and current at load side are listed in Table IV and the capacitor voltage balancing can be observed from Table V. Following conclusions can be drawn from Tables IV and V:

1) The CMC successfully creates the desired line-to-neutral and line-to-line voltage waveforms at its input;
2) The MSS applied in this work successfully balances capacitor voltages of CMC.



(a) (b)

Fig. 7 (a) line-to-neutral and (b) line-to-line voltages of CMC based T-STATCOM.

Table IV. Power factor, voltage and current analysis

	Power factor	Load voltage	Load current
Without proposed T-STATCOM	0.4705	542.6	45.22
With proposed T-STATCOM	1	776.2	64.68

Table V .Voltage difference between capacitors

	Between capacitors			
	C_1&C_2	C_2& C_3	C_3&C_4	C_4&C_5
Voltage	-0.02253	-0.02229	-0.0225	-0.02283

VI. CONCLUSION

A 11-level T-STATCOM system by the parallel use of five CMCs built in this work has been implemented primarily for the purposes of reactive power compensation and terminal voltage regulation and secondarily for power factor improvement. The Cascaded Multilevel Converter based T-STATCOM with MSS algorithm is simulated using MATLAB/SIMULINK. The primary purpose is met with compensation of reactive power required in line and the terminal voltage regulation is improved by increasing voltage from 542.6V to 776.2V. Here the power factor of system is improved from 0.4 to 1 with implementation of STATCOM in parallel to the line.

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