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Design of Low-Voltage, Power Proposed DynamicClocked Comparator

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Abstract- To maximize speed and power efficiency, use of dynamic comparators in high speed analog-to-digital converters.Analysis in this paper, the delay and power consumption of the dynamic comparators will be analyzed and logical expressions are derived. From the logical expressions, designers can obtain comparator delay and power consumption in dynamic comparator design. Based on the present analysis, a new comparator is proposed, where the circuit of a conventional double tail comparator is improved for low-power and fast performance even in minimumsupply voltages. The simulation results of three comparators shows that the proposed dynamic comparator will occupy less active area and also having higher speed and consumes less power. Post-layout simulation results in CMOS technology confirm the analysis results are 0.18-µm. It shown that in the proposed comparator both the power consumption and delay time are significantly reduced, while consuming power Upto 0.2 mW and 0.19 mW, respectively.

***General Term*-Double Tail comparator, dynamic latch comparator, high-resolution analog-to-digital converters (ADCs).**

I. INTRODUCTION

COMPARATOR is one of the most fundamental building blocks in analog-to-digital converters (ADCs). Many high speed ADCs, such as Successive adaptive ADCs, require high-speed, low power comparators with small chip area [1]. One such application where low power, high speed and maximumresolution are required is Analog-to-Digital Converters (ADCs) for mobile and portable devices.

The performance limiting blocks in suchADCs are typically inter-stage gain amplifiers andcomparators. Hence, designing high-speed comparators is more challenging when the supply voltage is minimum. Many techniques are available such as body boosting technique [2]which employs body driven transistor using dual oxide process[3], which can carry high supply voltage have to meet low voltage design challenges. Boosting and Boots trapping are two techniques based on boosting the supply, reference, or clock voltage to address input-range and switching problems.

In order to convert a small input-voltage difference to a full-scale digitallevel in a short time, they use positive feedback mechanism with pair of back-to-back cross coupled inverters (latch or sense amplifier). However, an input-referred latch offsetvoltage, resulting from static mismatches such as thresholdvoltage Vth and Cox variations in the regenerative latch deteriorates the accuracy of such comparators. Body-driven technique is adopted [4], thatremoves the threshold voltage requirement such that body drivenMOSFET operates as a depletion-type device.

If outsized devices are used for the latching stage, a low offset voltage can be achieved at the cost of the reduced speed due to slowing the regeneration time and the maximize power dissipation [5]. More basically, by using pre-amplifier the input-referred latch offset voltage can be reduced at preceding the regenerative output latch stage.It can amplify a minimum input voltage difference to a maximum enough voltage to overcome the latch offset voltage. However, due to the continuous time and technology scaling the preamplifier based comparators suffer not only from large power consumption for a large bandwidth but also from the reduced intrinsic gain with a reduction of the drain-to-source resistance [6].

In many low power applications comparator speed, power dissipation, power efficiency and number of transistors are more important. If comparator speed is more priority, then regenerative stage could be designed to start its operation from intermediatebetween power supply and ground, for consider, pre-amplifier based clocked regenerative comparator. However, the static power consumption is comparatively high.

If comparator was designed based on priority given to power reduction, then number of transistors increases so reduction incomparator speed, for example double tail latched comparator. Comparator design mainly depends

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on the target application. Even though, an input-referred latch offset voltage (hence offset voltage) [7], resulting from the device mismatch such as, current factor βand parasitic node capacitance , output load capacitance mismatch, threshold voltage Vth, limits the accuracy of the comparators.

Offset, along with power consumption which can be defined by the accuracy of comparators, ithas of keen interest in achieving overall effective performance ofADCs. In earlier, pre-amplifier based comparators have been used for ADC architectures in low power applications such as flash and pipeline. The main shortcoming of pre-amplifier based comparators is the high constant power consumption [8]. To overcome this issue, dynamic latch comparators are frequently used that make a comparisonfor every clock period and require much minimum power as compared to the pre-amplifier based comparators. However, these dynamic latch comparators suffer from large offsets making them less favorable in flash ADC architectures. In pipeline ADCs architecture, digital correction techniques with adequate over-range protection it can tolerate such large offsets.

II. CLOCKED REGENERATIVE COMPARATORS

Clocked regenerative comparators have found wide applications in many high-speed ADCs since they can make fast decisions due to the strong positive feedback in the regenerative latch. Recently, many comprehensive analyses have been presented, which investigate the performance of these comparators from different aspects, such as noise offset [9], [10] and random decision errors [11] and kick-back noise [12]. In this section, a complete delay analysis is presented; the delay time of two common structures i.e., conventional dynamic latch comparator and conventional dynamic double-tail comparator are evaluated, based on which the proposed comparator will be presented.

III. DYNAMIC LATCHCOMPARATOR

The dynamic latched comparator is composed of two stages as shown in Fig. 1. The first stage is the interface-intermediate stage which consists of all the transistors except two cross coupled inverters. The second stage is the regenerative stage that is covered of the two cross coupled inverters, whereat eachstage input is connected to the output of the other. It operates in two phases i) Interface phase and ii) Regeneration phase. It has single NMOS tail transistor connected to ground (Vss). When clock is low (clk=0) tail transistor is turns off and depending on Vp and Vn output reaches to VDD or gnd, if Vp>Vn output of Vp discharge faster than output of Vn. When clock is high (clk=Vdd) tail transistor is turns on and both the outputs discharges to ground.

This is methods of reducing power and delay in dynamic latch comparator circuit over the double tail comparator and pre-amplifier based comparators. Double tail comparator has minimum power consumption but has low speed because of more stacked transistor count but in pre-amplifier based clocked comparator has high speed because of minimum stacked transistor count but power consumption is more, it consumes static power consumption during the amplification period However, since high frequency required for pre-amplifier based clocked comparator is to work , the power consumption of the pre-amplifier based clocked comparator becomes comparable to the double tail based latch comparator. Hence the performance and efficiency of the pre-amplifier based clocked comparator is limited by the static power dissipation in the interface or regeneration phase.
Due to fast speed, high input impedance, full-swing output and low power consumption,dynamic latch comparators are very outstanding for many low power applications such as high-speed analog-to-digital converters (ADCs), data receivers and memory sense amplifiers (SAs). They use positive feedback mechanism with a pair of back-to-back cross coupled inverters (latch or amplifier) in order to convert a trivial input-voltage difference to a full-scale digital level in a small time. Therefore dynamic latch comparator is more suitable for both high speed and low power dissipation because of decrease in stacked transistor count which overcomes the issue of double tail latch and pre-amplifier based clocked comparators.

Since by using known techniques, the comparator offset voltage can be reduced, the main attention of this paper is the comparator speed, power dissipation and dies area. Simulation result of comparing the power dissipation versus the supply voltage and delay versus the supply voltage of the comparator at 1.1V supply.

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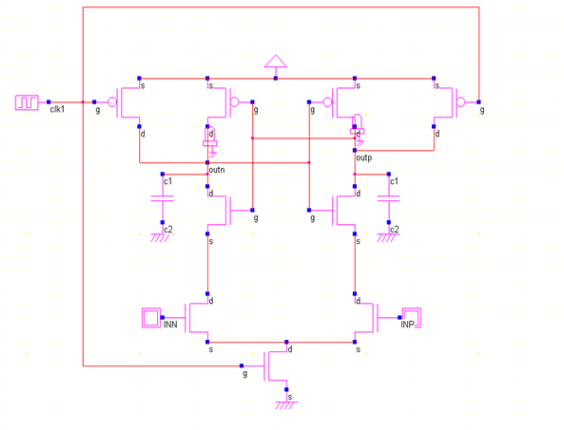

Fig 1 Schematic of Dynamic latched comparator

The results show that the dynamic latch comparator outperforms then other 2. Henceforth the 3 comparators will be compared. The layouts are automatically extracted and simulated by using micro wind simulator. Shows simulation results of the power dissipation, delay versus supply voltages (Vdd) respectively for the 3 designs. Compare to other 2 design the results show that the dynamic latch comparator circuit has less delay time and less power dissipation.

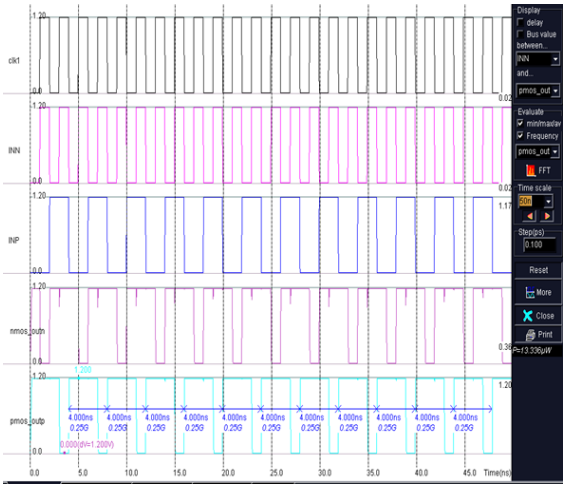

Fig 2 shows Simulation Result of Dynamic Comparator

IV. DOUBLE TAIL COMPARATOR

The operation of the double tail comparator is as follows. During the reset phase when CLK = 0 and Mtail is turns off, reset transistors (M7–M8) takes both output nodes Outn and Outp to VDD to define a initial condition and to have a valid logical level during reset.

In decision making phase, when CLK = VDD, transistors M7 and M8 are turns off, and Mtail is turns on. Output voltages, which had been pre-charged to VDD, start to drops with different discharging rates depending on the corresponding input voltage(INN/INP). Assuming the cases supposeVINP > VINN, Outp discharges faster than Outn based on the input, hence when Outp reaches or falls down to VDD–|Vthp|before Outn (discharged by transistor M1), thecorresponding pMOS transistor (M5) will turns on initiating thelatch regeneration operation caused by back-to-back inverters (M3, M5 Transient simulations of the conventional double tail comparator for input voltage difference of _Vin = 5 mV, Vcm = 0.7 V, and VDD = 0.8 V and M4, M6). Thus, Outn taken to VDD and Outp discharged to ground. If VINP < VINN, the circuits works vice versa. A conventional double-tail comparator is shown in Fig 3. This topology has less stacking transistor and therefore can operate in low offset voltage. Input-dependentdifferential voltage _Vfn(p) will build up. The intermediatestage formed by MR1 and MR2 passes _Vfn(p) to the cross coupledinverters and also provides a good defending between input and output, resulting in reduced value of kickback noise [10].

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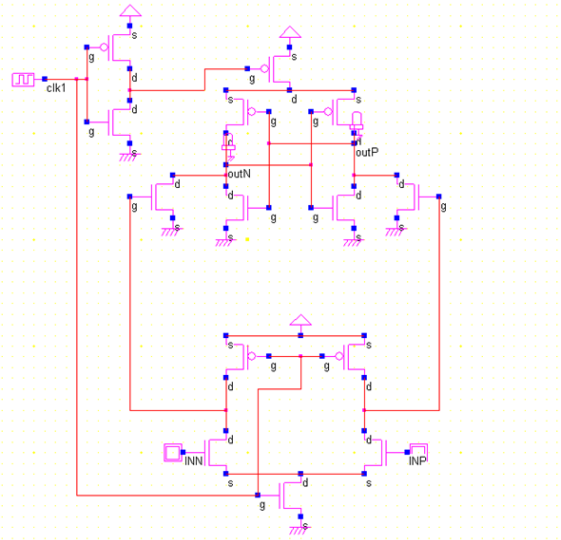

Fig 3 Shows Double Tail Comparator

Similar to the conventional dynamic latch comparator, the delay of this comparator comprises two main parts,

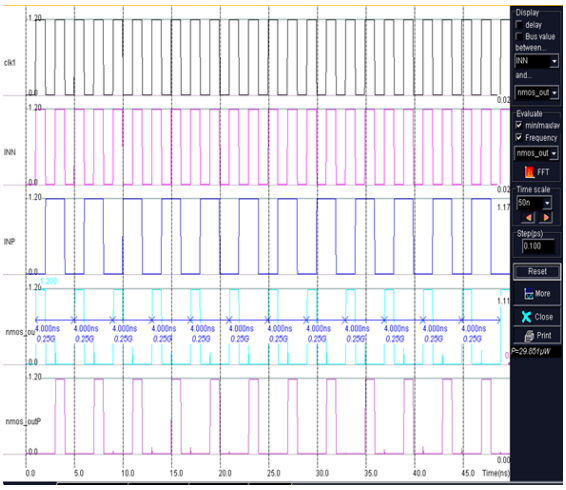

Fig 4 Shows Simulation Result of Double Tail Comparator

t0 and tlatch. The delay t0 represents the load capacitance CLout 0f capacitive charging (at the latch stage output nodes are Outn and Outp) until the first n-channel transistor (M9/M10) turns on, after which the latch regeneration operation starts; thus t0 is obtained

V. PROPOSED COMPARATOR

The operation of the proposed comparator is as follows. During reset phase (CLK = 0, Mtail1 and Mtail2 areturned off, avoiding static power), M3 and M4 pulls both the node fn and fp toVDD, hence transistor Mc1 and Mc2 are turns off. Transitional stage transistors, MR1 and MR2, reorganize both latch outputs to ground. During comparison -making phase (CLK = VDD, Mtail1, and Mtail2 are turns on), transistors M3 and M4 are turns off. Moreover, at the beginning of this stage, the control transistors are still off (since fn and fp are proximateVDD). Thus, fn and fp starts to discharge with different rates according to the input voltages. Suppose VINP > VINN, thus fn discharge faster than fp, (since M2 delivers more current than M1). As long as fn continues dropping, the corresponding pMOS control transistor (Mc1 in this case) starts to turns on, pulling fp node back to the VDD; so another control transistor (Mc2) remains off, allowing fn to be discharged Completely. Hence, by the time passing, the difference between fn and fp (_Vfn/fp) increases in an exponential

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manner, leading to the reduction of latch regeneration time. Despite the effectiveness of the proposed idea, one of the points which should be considered is that in this circuit,

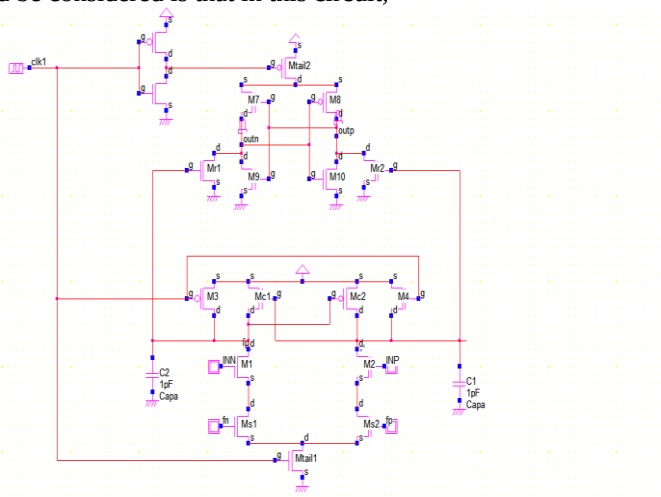

Fig 5. shows Proposed Comparator

it generates internal capacitor itself, so it can operate at minimum offset voltage, power can be reduced Upto 0.106mw .when one of the control transistors (e.g., Mc1) turns on,a current from VDD is drained to the ground via input and Mtail transistor (e.g., Mc1, M1, and Mtail1), resulting in static power Consumption. To overcome this issue, two nMOS switches are placed below the input transistors.The transitional stage formed by MR1 and MR2 passes -Vfn(p) to the cross coupled Inverters and also affords a good guarding between input and output, resulting in reduction of kickbacknoise.At the beginning of the comparison making phase, due to the fact that both fn and fp nodes have been pre-charged to VDD.(During the reset phase), both switches are closed and fn and fp start to discharge with different rates. As soon as the comparator detects that one of the fn/fp nodes is discharging faster, Control transistors will act in a way to increase their voltage difference.

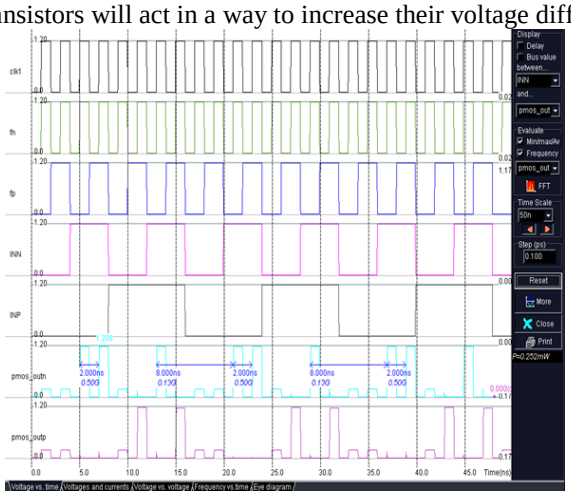

Fig 6 Shows simulation of the proposed comparator

For input voltage difference of _Vin = 5 mV, Vcm = 0.7 V, and VDD = 0.8 V. Suppose that fp is pulling up to the VDDand fn should be discharged completely, hence the switch in the charging track of fp will be opened (in order to prevent any current drawn from VDD) but the other switch connected to fn will be closed to allow the complete discharge of fn node.

TABLE I. PERFORMANCE COMPARSION

Technique used	Power consumption (mW)	Delay (ns)	Time (ns)
Dynamic Latched Comparator	0.335mW	4.0ns	5ns

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Double tail Comparator	0.295mW	4.0ns	5ns
Proposed Comparator	0.106mW	2.0ns	5ns

VI. CONCLUSION

In this paper, we presented a inclusive delay analysis for clocked dynamic comparators. Two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators were analyzed. Also, based on the analyses, a new comparator is proposed with low-voltage low-power capability was proposed in order to improve the performance of the Comparatorcircuit. Thedelay and energy per conversion of the proposed comparator is reduced to a maximumextent in comparison with the conventional dynamic comparator and double-tail comparator.It can be implementing successfully in successive Adaptive Converter in very efficient manner.

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