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A Novel Design Approach to Achieve Fault Coverage in Sequential Circuits

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Abstract-In the design of sequential circuits, to avoid the excess time required for testing, the testable sequential circuits based on conservative logic gates using reversible logic are presented here which can be tested for unidirectional stuck-at faults using only two test vectors- all 1s and all 0s. The testable latches, master-slave flip-flops and double edge triggered flip-flops are designed using Fredkin gate and the fault coverage is calculated. Thus the proposed sequential circuits based on conservative logic gates outperform the conventional sequential circuits in terms of testability. A new conservative gate called multiplexer conservative QCA gate is presented which overcomes Fredkin gate in terms of complexity and area.

Index terms- **Conservative logic, fault coverage, Quantum dot Cellular Automata (QCA), reversible logic.**

I. INTRODUCTION

A stuck-at fault is a particular fault model in which individual signals or pins are assumed to be stuck at either logic 1 or logic 0. These single missing or additional faults of sequential circuits can be detected by only two test vectors using a conservative reversible Fredkin gate .i. e, by setting all inputs to 1s and then by consequent checking of outputs for the occurrence of any 0s, stuck-at-0 faults can be detected. Similarly, by setting all inputs to 0s and then by consequent checking of outputs for the occurrence of any 1s, stuck-at-1 faults can be detected.

Reversibility is the property of circuits in which there is a dependency between the input and the output vectors, that is, distinct input states always lead to distinct output states.Conservative logic is a logic family that shows the property that there are an equal number of 1s in the inputs as there are in the outputs. Conservative logic may be reversible in nature or may not be reversible in nature. Conservative logic is also known as reversible conservative logic when there is a one-to-one mapping between the inputs and the outputs states and also when there are equal numbers of 1s in the inputs as in the outputs. If one-to-one composition between the inputs and the outputs vectors is not maintained, conservative logic circuits are not reversible. In reversible logic, the state of the computational device just prior to an operation is uniquely determined by its state just after the operation. In other words, no informationabout the computational state is lost. From a thermodynamic point of view, it is showed that kTln2 energy dissipation would not occur, if a computation is done in a reversible way. There are evolving nanotechnologies, such as quantum-dot cellular automata (QCA), where the energy dissipated due to information destruction will be a significant factor of the total heat dissipation of the system.

The proposed design of testable sequential circuits based on conservative logic gates will take care of the fan-out (FO) at the output of the reversible latches and can also disorder the feedback to make them fit for testing by only two test vectors, all 0s and all 1s. i.e., while executing, circuits will have feedback. However, to detect faults in the test mode, proposed technique will disrupt feedback to make them testable as combinational circuits. This technique is then used to provide the design of testable master-slave flip-flops and double edge triggered (DET) flip-flops. The reversible design of the DET flip-flop is proposed for the first time in the literature. Also fault is injected into the DET flip-flop and the corresponding output is compared along with the original one thus obtaining the fault coverage in the circuit. Further, a new conservative logic gate called multiplexer conservative QCA gate (MX-cqca) is proposed that is non-reversible but conservative in nature and is analogous to the Fredkin gate of working as 2:1 multiplexer. The proposed MX-cqca gate beats the Fredkin gate based on complexity, speed, and time. The rest of this paper is organized as follows. Section II presents the related work that has already done. Section III provides the design of testable reversible latches; Section IV describes design of testable reversible master-slave flip-flops, while Section V presents design of testable

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Volume 3, Issue 1, January 2014

reversible DET flip-flop. Section VI provides the proposed multiplexer conservative QCA gate and the simulation results are given in section VII.

II. RELATED WORK

The techniques for the construction of reversible circuits that realize the functionality of any given arbitrary digital circuit, including a two-input lookup table (LUT), and automatically translating the above-mentioned reversible circuits into online testable circuits are presented in [1]. In essence, the problems of low power design and online error detection are collectively discoursed in this paper.Nevertheless; offline testing of faults in reversible sequential circuits is not discussed here. As per [2], a class of novel designs based on conservative reversible logic for the construction of concurrently testable sequential circuits for molecular QCA is proposed. The single missing or the additional cell defect in QCA of the conservative reversible Fredkin gate is studied. Designs for concurrently testable latches (*D* latch, *T* latch, *JK* latch, and *SR* latch) are presented using Fredkin gate, and is applicable in molecular QCA, which is the main contribution of this paper. However, these designs are not synchronously testable. According to [3], to facilitate the conversion of sum-of-products(SOP) expressions into reduced majority logic, a Boolean algebra based on a geometrical interpretation of three variable Boolean functions is explained. All possible three-variable Boolean functions are represented by the introduction of thirteen standard functions. For each of these standard functions, reduced majority expression is specified. A QCA adder design is depicted, and showed that the total hardware can be minimized by the proposed method, when compared to previously published designs.

A. Conservative reversible Fredkin gate

The Fredkin gate is a widely used reversible conservative logic gate, which was first proposed by Fredkin and Toffoli in [5]. The Fredkin gate shown in Fig. 1 can be described as a mapping (A, B, C) to ($P = A$, $Q = A\_B + AC$, $R = AB + A\_C$), where A, B, C are the inputs and the outputs being P, Q, R. The truth table for the Fredkin gate is shown in [4], which exhibits that Fredkin gate is conservative and reversible in nature, that is, it has unique input and output mapping and also has the equal number of 1s in the inputs as in the outputs. It is known as 3*3 gate because it has 3 inputs and 3 outputs.

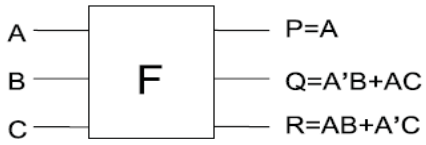

Fig. 1 Fredkin gate

B. Basics of QCA computing

In this paper, the proposed multiplexer cqca gate is implemented based on the QCA nanotechnology, thus an introductory material on QCA computing is provided here. QCA is one of the emerging nanotechnologies in which it is possible to implement reversible logic gates [2]. QCA makes it possible to achieve circuit densities and clock beyond the limits of existing CMOS technology.

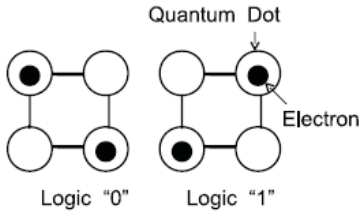

Fig. 2 QCA cell as logic 1 and logic 0

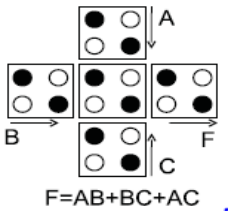

Fig. 3 Majority gate (MV)

A QCA cell is a coupled dot system in which four dots are at the vertices of a square. The two extra electrons of the cell, occupy the diagonals within the cell. Fig. 2 shows the four quantum dots in a QCA cell and the implementation of logic 0 and logic 1 in a QCA cell, respectively. The basic QCA gate is the MV or the majority gate which is shown in Fig. 3 and is represented as $F = AB + BC + AC$, where F is the majority of the inputs A, B, and C.

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III. DESIGN OF TESTABLE REVERSIBLE LATCHES

A. Design of Testable Positive Enable Reversible D Latch

The characteristic equation of the D latch is given by $Q+ = D \cdot E + \bar{E} \cdot Q$. In this work, enable (E) refers to the clock and is used interchangeably in place of clock. When the enable input (clock) is 1, the value of the input D is obtained at the output that is Q+ = D. While, when E = 0 the latch upholds its previous state, that is Q+ = Q. The characteristic equation of the D latch can be mapped to the Fredkin gate (F). Fig. 4(a) shows the realization of the reversible D latch using a single Fredkin gate. But fan out (FO) cannot be allowed in conservative reversible logic. Moreover, this design cannot be tested for our required purpose of using only two test vectors because of the feedback, as the output Q may latch 1 if the inputs are toggled from all 1s to all 0s which could be misinterpreted as stuck-at-1 fault.

In this paper, another Fredkin gate is cascaded to the output Q as shown in Fig 4(b). C1 and C2 are the two control signals in the design. The design can work in two modes: 1) Normal mode and 2) Test mode.

1) *Normal Mode*: The normal mode is shown in Fig. 4(c) in which given$C1C2$ = 01 and the design will be working as a D latch without any fan-out problem.

2) *Test Mode*: In test mode, when $C1C2$ = 00 as shown in Fig. 4(e) it will make the design testable with all 0s input vectors and output T1 and T2 will become 0 resulting in making it testable with all 0s input vectors. Thus, the presence of any stuck-at-1 fault can be detected. When $C1C2$ = 11 as shown in Fig. 4(d), the output T1 and T2 will become 1 and the design can be tested withall 1s input vectors for any stuck-at-0 fault. It can be seen that C1 and C2 will disrupt the feedback intest mode, and can take care of the fan out in the normal mode.Thus, the proposed design works as a reversible Dlatch and can be tested with only two test vectors, for any stuck-at fault by utilizing the inherent property of conservative reversible logic.

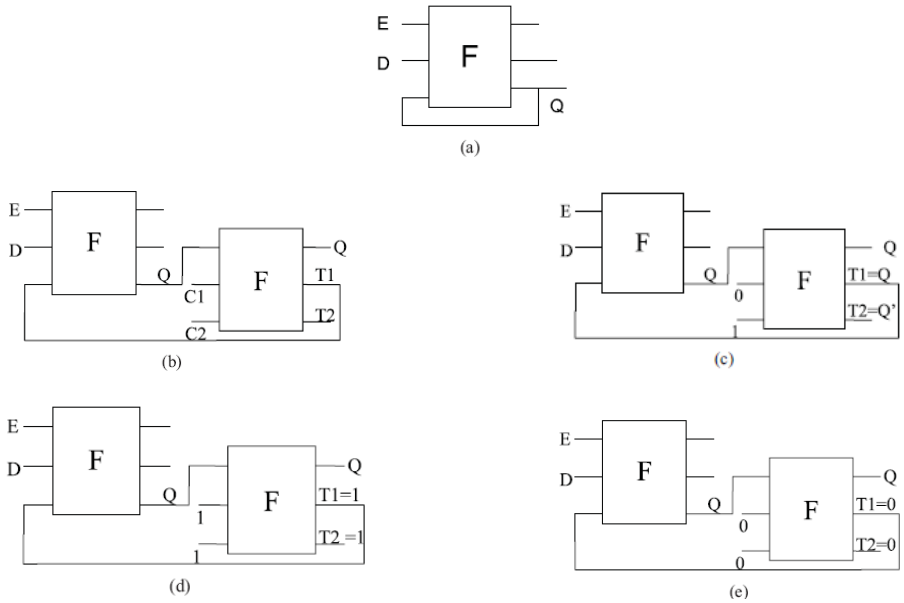

Fig. 4 Design of testable reversible D latch using Fredkin gate. (a) Fredkin gate based D latch. (b) D latch with control signals C1 and C2. (c) Normal mode: $C1$ = 0 and $C2$ = 1. (d) Test mode for stuck-at-0 fault: $C1$ = 1 and $C2$ = 1. (e) Test mode for stuck-at-1 fault: $C1$ = 0 and $C2$ = 0.

B. Design of Testable Negative Enable Reversible D Latch

We have already seen the positive enable reversible D latch. A reversible D latch that can pass the input D to the output Q when E = 0; otherwise remains the same state is negative enable. The negative enable D latch has its characteristic equation given by $Q+ = D \cdot \bar{E} + E \cdot Q$.

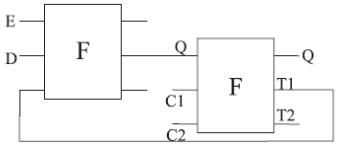

Fig. 5 Fredkin gate-based negative enable testable D latch

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Volume 3, Issue 1, January 2014

In the negative enable D latch, characteristic equation is mapped on the second output of the Fredkin gate as shown in Fig. 5. The second Fredkin gate in the design plays a major role in making the design testable by only two test vectors, all 0s and all 1s, as illustrated above for positive enable reversible D latch. The negative enable D latch is helpful for the design of testable reversible master-slave flip-flops. This is because in the testable reversible master-slave flip-flop, it can work as a slave so that no clock inversion is required. It will be discussed in detail in the following section.

IV. DESIGN OF TESTABLE MASTER-SLAVE FLIP-FLOPS

The master-slave strategy of using one latch as a master and the other latch as a slave is used to design the reversible flip-flops in the existing literature. In this paper, the design of testable flip-flops using the master slave strategy is presented that can be tested for any stuck-at faults using only two test vectors, all 0s and all 1s. The design of the master-slave D flip-flop is shown in Fig. 6, in which we have used positive enable Fredkin gate-based testable D latch as the master latch, while the negative enable Fredkin gate-based testable D latch as the slave latch. The testable reversible D flip-flops has four control signals *mC*1,*mC*2, *sC*1, and *sC*2. *mC*1 and *mC*2 are the control the modes for the master latch, while *sC*1 and *sC*2 control the modes for the slave latch. In the normal mode, for this design of master-slave flip-flop, the values of the controls signals are *mC*1 = 0 and *mC*2 = 1, *sC*1 = 0 and *sC*2 = 1, as similar to the values of the control signals C1 and C2 for the testable D latches.

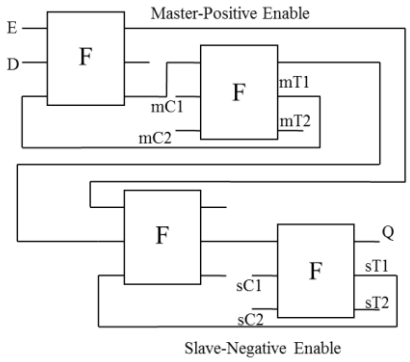

Fig. 6 Fredkin gate-based testable reversible master-slave D flip-flop.

In the test mode,

1) To design the circuit with all 0s testvector for detecting any stuck-at-1 fault, the values of the control signals are mC1=0 and mC2=0, sC1=0 and sC2=0.This will make the outputs *mT*1 and *sT*1 as 0, which breaks the feedback and the design becomes testable with all 0s input vectors for any stuck-at-1 fault.
2) To design the circuit with all 1s input vectors for detecting any stuck-at-0 fault, the values of the control signals aremC1=1 and mC2=1, sC1=1, and sC2=1. This result in outputs mT1 and sT1 having a value of 1, which breaks the feedback and results in the design testable with all 1s input vectors for any stuck-at-0 fault.

The master-slave flip-flops can also be implemented using T flip-flops, JK flip-flops, and SR flip-flops similarly in which master is designed using the positive enable corresponding latch, while the negative enable Fredkin gate-based D latch can be used to design the slave.

V. DESIGN OF TESTABLE REVERSIBLE DET FLIP-FLOPS

The DET flip-flop can receive input signals at two levels of clock. This flip flop can be used to sample and store the input data at both the edges, i.e., at both the rising and falling edge of the clock. The most popular way of designing the flip flop is the master slave strategy. In this work, *E* refers to the clock and can be used instead of clock. In the negative edge triggered master-slave flip-flop when *E* = 1, the master latch passes the input data while the slave latch remains in the storage state. When *E* = 0, the master latch is in the storage state while the slave latch passes the output of the master latch to its output. Thus, the flip-flop waits for the next rising edge of the clock to latch the data at the master latch and it does not sample the data at both the clock levels.

To overcome the above problem, the concept of DET flip flops have been introduced, which sample the data at both the edges. Thus, two data values can be received and sampled by DET flip-flop in a same clock period so that the frequency of the clock can be reduced to half of the master-slave flip flop while maintaining the same data rate. The DET flip-flop is designed by connecting in parallel the two latches, viz., the positive enable and the negative enable instead of series connection. A 2:1 MUX is connected at the output of the DET flip flop

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ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 3, Issue 1, January 2014

which transfer the output from one of these latches which is in the storage state (is holding its previous state). The equivalent testable reversible design of the DET flip flop is proposed in this paper and is shown in Fig. 7(a).

In the design of testable reversible DET flip-flop, the positive enable testable reversible D latch and the negative enable testable reversible D latch are arranged in parallel. The Fredkin gates labelled as 1 and 2 forms the positive enable testable D latch, while the negative enable testable D latch is formed by the Fredkin gates labelled as 3 and 4. The Fredkin gate labelled as 6 is used to copy the input signal D since FO is not allowed in reversible logic. The Fredkin gate labelled as 5 works as the 2:1 MUX and transfer the output from one of these testable latches (negative enable D latch or the positive enable D latch) that is in the storage state to the output Q. In this design, the testable positive enable D latch have the control signals pC1 and pC2, while nC1 and nC2 are the control signals of the testable negative enable D latch. Depending on the values of these control signals, the testable DET flip-flops work either in normal mode or in the test mode.

1) *Normal Mode*: The normal mode of the DET flip flop is demonstrated in Fig. 7(b) in which the control signal values are pC1 = 0, pC2 = 1, nC1 = 0, and nC2 = 1. The output of the positive enable D latch is thus copied by the help of pC1=0, pC2=1, thereby avoiding the FO, whereas nC1=0 and C2=1 helps in copying the output of the negative enable D latch thereby avoiding the FO.

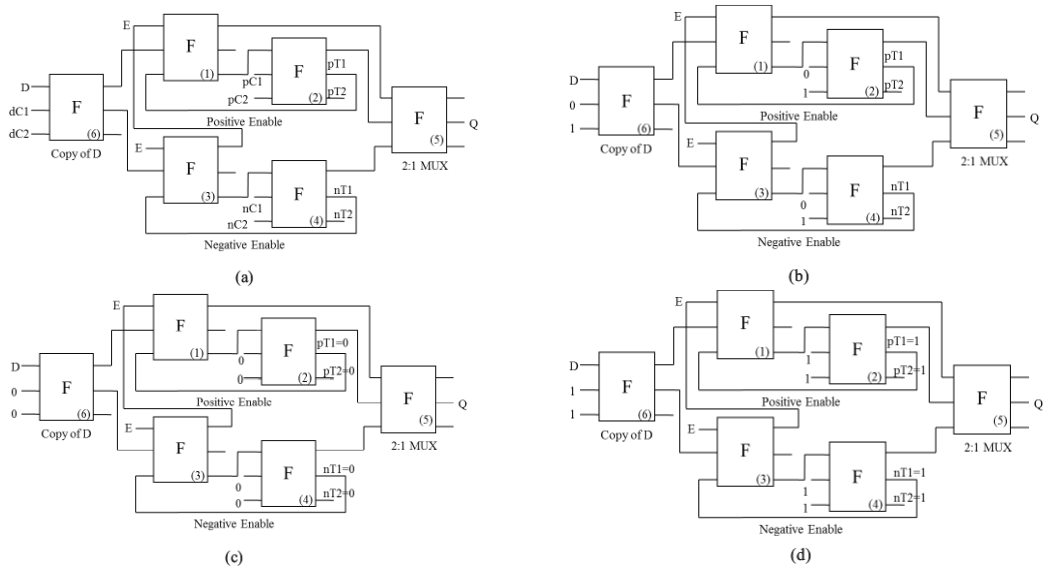

Fig. 7 Design of testable reversible DETflip-flop (a) Design of DET flip-flop using Fredkin gate. (b) Normal mode. (c) Test mode with all 0s testvector. (d) Test mode with all 1s test vector.

2) *Test Mode*: Two test modes are there.

a) *All 1s Test Vectors:* This mode is shown in Fig. 7(d) in which control signals will have values as all 1s.i.e.,pC1 = 1, pC2 = 1, nC1 = 1, and nC2 = 1. The pC1 = 1and pC2 = 1 will breaks the feedback of the positive enable D latch, whereas the feedback of the negative enable D latch can be broken by the help of nC1=1 and nC2=1. This makes the circuit testable for the presence of any stuck-at-0 fault by all 1s test vector.

b) *All 0s Test Vectors:* In this mode, the control signal values are pC1=0, pC2=0, nC1=0, and nC2=0 which is as shown in Fig. 7(c). The feedback of the positive enable D latch can be broken by pC1=0 and pC2=0 whereas nC1=0 and nC2=0 will helps in breaking the feedback of the negative enable D latch. This makes the design testable for the presence of any stuck-at-1 fault by all 0s test vectors.

VI. PROPOSED MULTIPLEXER CONSERVATIVE QCA GATE

In most of the designs, the designers will be in more interest in exploiting the testing advantages of conservative logic as well as saving the number of QCA cells. Thus, a new conservative logic gate is proposed in this paper that is conservative in nature is irreversible.

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Volume 3, Issue 1, January 2014

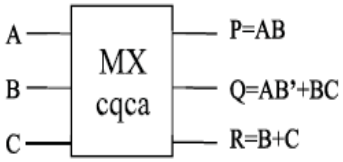

Fig.8 Proposed MX-cqca gate

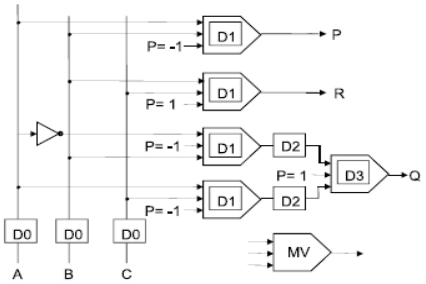

Fig.9 Design of MX-cqca gate using QCA

Table. I Truth table of MX-cqca gate

A	B	C		P	Q	R
0	0	0		0	0	0
0	0	1		0	0	1
0	1	0		0	0	1
0	1	1		0	1	1
1	0	0		0	1	0
1	0	1		0	1	1
1	1	0		1	0	1
1	1	1		1	1	1

The proposed conservative logic gate has three inputs and three outputs and is called multiplexer conservative logic gate (MX-cqca). One of the outputs of the MX-cqca gate is working as a multiplexer, whereas the other two outputs work as AND and OR gates. The mapping of the inputs to outputs of the MX-cqca is given by: $P = AB$; $Q = AB'+BC$; $R = B + C$, where A, B, and C are the inputs and the outputs being P, Q, and R, respectively. The block diagram of the MX-cqca gate is shown in Fig. 8. Table I gives the truth table of the MX-cqca gate. The table verifies that the number of 1s in the inputs is equal to the number of 1s in the outputs, i.e., the conservative nature of the gate. Fig. 9 shows the QCA design of the proposed MX-cqca gate. In the QCA design, we can see that the proposed MX-cqca gate requires four clocking zones and five majority gates for its QCA implementation. The comparison between the proposed MX-cqca gate and the Fredkin gate in terms of area and number of QCA cells can be performed and the results are included in the section of simulation results. Thus it concludes that MX-cqca is better than the existing Fredkin gate for implementing multiplexer-based designs.

VII. SIMULATION RESULTS

The simulation results are obtained using Modelsim and Xilinx and the coding is done by VHDL. The DET flip flop is first of all simulated using Modelsim and the corresponding waveform is shown in Fig.10.Four control signals pc1, pc2, nc1, nc2 are there and correspondingly four test output signals pt1, pt2, nt1, nt2 are also there which together constitute the normal mode and the test modes. When all 0s are given as input, the output thus obtained is used to detect any stuck at 1 faults that may have occurred whereas the all 1s when given as input, the corresponding output will be used to identify the stuck at 0 faults.

Fault coverage is defined as the measure of the ability of a test to detect a given fault that may occur on the device under test. That is, the total number of faults detected with the possible faults. For this, a fault is injected to the DET flip flop circuit and the corresponding changes are compared and then the fault can be detected. The output for the fault coverage in DET flip flop is depicted in Fig.11. A table containing the input vectors, expected output vectors and the fault patterns is shown here in Table II. The fault patterns are obtained after injecting the fault into the circuit and it is compared against the expected output vector. By comparing with the expected output vector, stuck at 1 faults as well as stuck-at 0s are obtained. Here single stuck at faults can be easily identified. A bit change will be detected using this fault injection method and the fault coverage is estimated.

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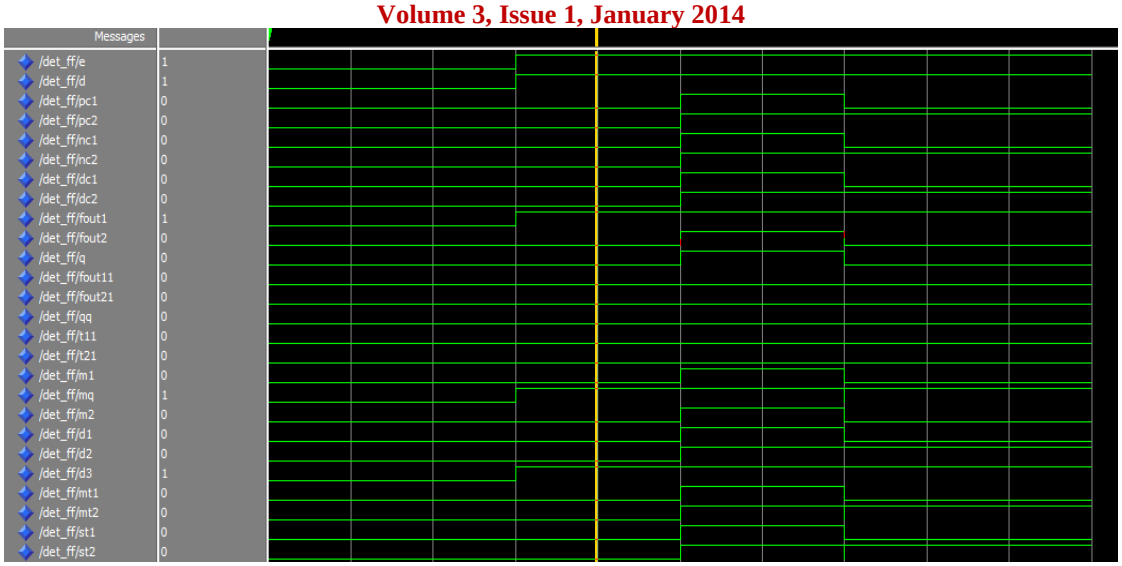

Fig. 10 Output of reversible DET Flip flop

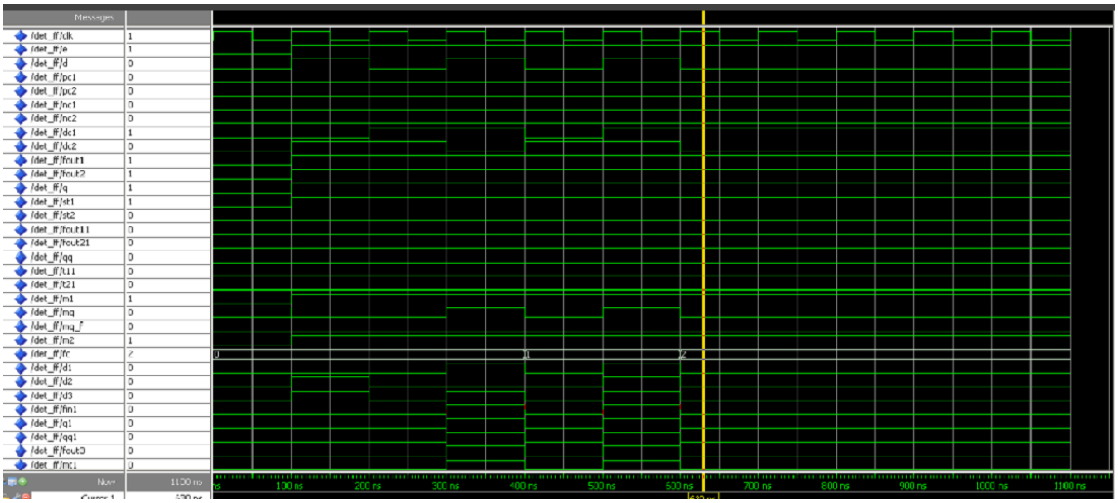

Fig.11 output for fault coverage

Table. II Table showing fault coverage

Input vector	Expected Output Vector	Fault Patterns
001	000	010—s-a-1
101	010	000—s-a-0
111	111	101—s-a-0
000	000	010—s-a-1

MX-cqca gate is implemented using QCA logic. The basic gate used in the QCAis the majority gate (MV). So here, using five MVs, MX-cqca gate is implemented and the corresponding simulation result is demonstrated in Fig.12.

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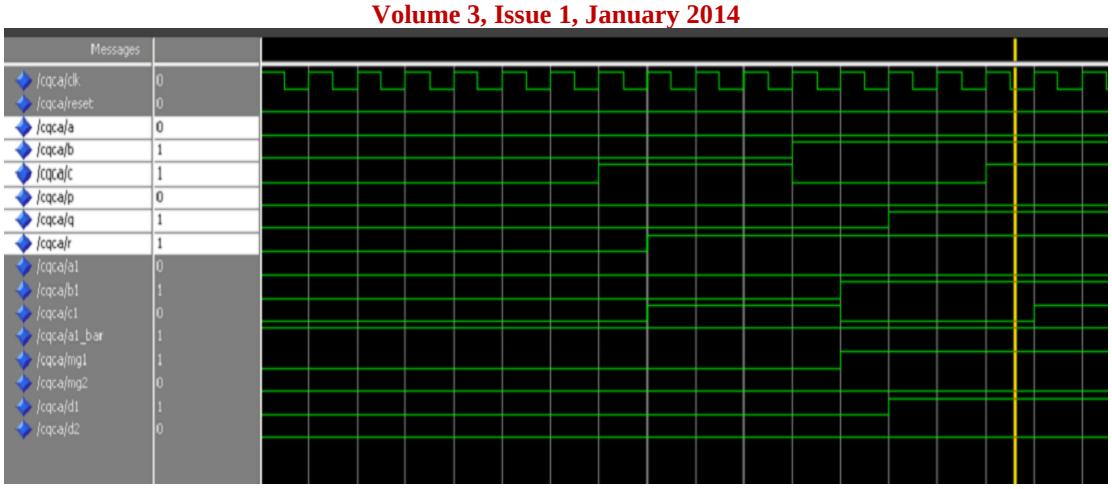

Fig.12 output of MX-cqca gate

Table. III. Comparison of Fredkin and MX-cqcagates

	Fredkin gate	MX-cqca
MVs	6	5
Clock Zs	4	4
Total cells	246	218

The comparison of the Fredkin gate and the MX-cqca gate is shown in the Table III.

VIII. CONCLUSION

The reversible sequential circuits based on conservative logic that is testable for any unidirectional stuck-at faults using only two test vectors, all 0s and all 1s is proposed here. The proposed sequential circuits based on conservative logic gates outclass the sequential circuit implemented in conventional gates in terms of testability. Also as the complexity of a sequential circuit in terms of number of gates increases, the number of test vectors needed to test the sequential circuit also increases. Thus, the significance of the proposed conservative reversible sequential circuits compared to the conventional sequential circuit is the need of only two test vectors to test any sequential circuit regardless of its complexity. The fault coverage is then calculated. Finally, Fredkin gate and MX-cqca gate are compared and the latter is found to perform well in terms of area and complexity.

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