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Soft Error Reduction of Logical Circuits by Using RAR Methodology

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Abstract-Due to shrinking feature sizes and decreasing supply voltages in current technology scaling trends, the reliability of circuit would be affected by radiation induced particle hits. Nowadays soft errors are main factor in reliability degradation of logic circuits, which have been a great concern in memories also. Here, we present a systematic and integrated methodology for circuit robustness to soft errors. Based on redundancy addition and removal (RAR) method, our proposed work explains that the soft error rate (SER) reduction framework provides eliminating those gates by means of large support to the complete SER. The plan called resizing is included into our framework, as post-RAR additive SER optimization. We can minimize area and power overheads by identifying most critical gates to be upsized while continuing a high level of soft error toughness.

Index Terms: **Mean Masking Impact (MMI), Single event transient, soft error rate, mean Error Impact (MEI).**

I. INTRODUCTION

In the deep sub micrometer design the circuit reliability has become a critical issue. Reliability degradation of the logic circuits by currently some of the main factors like crosstalk, voltage drop, and radiation induced transient errors. Digital designs are becoming more susceptible to radiation-induced particle hits resulting from radioactive decay and cosmic rays, than all other factors by the effect of current scaling technology trends. Glitch or single-event transient occurs when a low-energy particle that before had no effect on a circuit can now flip the state of a storage node. When SET is propagated to an output and latched into a memory element it is referred as soft error or single-event upset. The rate at which soft errors occur is called soft error rate (SER). There are three mechanisms that offer logic circuits with effective protection against soft errors while SET propagation.

Logical masking A portion of the combinational logic that is blocked from affecting the output when a particle strikes occurs it is mainly because of a subsequent gate whose outcome is entirely determined by its other input values.
Electrical Masking happens when pulse is attenuated by subsequent logic gates and it is resulting from a particle strikeas a result of the electrical properties of the gates to the point that the result of the circuit is does not affected by these properties.
Latching-Window Masking takes place when the pulse reaches a latch resulting from a particle strike, but not at the clock transition where the latch captures its input value.

However, these three mechanisms prevent some SETs from being latched and alleviate the effects of soft errors in digital systems it will affect by continuous scaling trends. Logical masking is decreased due to decreasing logic depth. Electrical masking is decreased due to faster logic gates, lower supply voltages and smaller node capacitance. Latching-window masking is decreased due to increasing clock frequencies. Soft errors can be alleviated in memories by using conventional error detecting codes and correcting codes. Usually two types of methods are used for soft error hardening. The first one, **fault avoidance**, where effect of SET generation can be reduce when minimizing the happening of SETs at the most sensitive nodes. This category works on the device level where charge collection can be reduce by exploiting fabrication process. So, a baseline circuit has less effect to harmful particle hit or no damage to the radiation-hardened version. The second one, **fault correction**, here can reduces the possibility of generated SETs being latched through maximize the probabilities of three masking mechanisms. In second category the SER improvement can achieve through circuit level or higher levels of abstraction. In this paper, we suggest a procedure belonging to the fault correction.

A. Related Work

As presented in [1] for combinational circuits introduce a methodology called logic-level soft error mitigation. The proposed technique is based on selective addition of appropriate functionally redundant wires and exploits the existence of logic effects in design to the circuit. Here, plan the necessary conditions for adding candidate

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functionally redundant wires and talk over three methods for identifying them to the circuit. This paper evaluates the SET sensitization probability reduction based on an algorithm that achieved by candidate functionally redundant wires, and when added to the design, minimizes its SER selects an appropriate subset. As suggested in[2] during soft error analysis and logic synthesis examines the use of partial truth tables generated through bit-parallel functional simulation. Here first present, integrates tools for the logic-level Analysis of Soft Error Rate by a signature-based CAD context and then Signature-based Design for Reliability (SiDeR).Then observe that the soft error rate (SER) of a logic circuit is closely related to various testability parameters, such as signal observability and probabilities are closely related to the soft error rate (SER) of a logic circuit and also demonstrates that these parameters can be computed very efficiently through signatures. In [3], the proposed method based on the use of binary decision diagrams (BDDs) and algebraic decision diagrams (ADDs) for the unified symbolic analysis of circuit reliability in ordered to estimate the susceptibility to errors in combinational logic. A context that enables the analysis of combinational circuit reliability by using different aspects such as output exposure to error, impact of each gates on individual outputs and the reliability of circuit dependence on duration of glitch, amplitude, and input patterns.

II. SYMBOLIC SER ANALYZER

In this section error impact and masking impact of each gate can be calculated concurrently in combinational logic. The following events can be defined in ordered to model a transient glitch originating at gate to be latched at output,

A: Correct output is "0" (if A$\geq V_s$) or Correct output is "1" (If A $<V_s$)where V_s is the switching threshold of the latch and A is the amplitude of the glitch.

D: t_{setup} + t_{hold}< D where, t_{setup} and t_{hold} are the setup and hold times of the latch and D is the duration of the glitch.

T: t ∈ [T +t_{hold} - t_p– D, T –t_{setup}-t_p] indicates the time when the initial glitch occurs, t_p is the propagation delay from gate 'G' to output 'F', and T is the moment of a latch trigger.

These three events are necessary conditions for a soft error to takes place. The probability that a soft error occurs can be derived as,

$$P(A \cap D \cap T) = \sum_K \left(\frac{D_{k-}(t_{setup}+t_{hold})}{T_{clk}-d_{init}} \cdot P(D = D_K) \right) \quad (1)$$

Where,

D_K – Set of possible glitch duration

T_{clk} – Clock period

D_{init} – Uniformly distributed in the interval

Binary decision diagrams (BDDs) and algebraic decision diagrams (ADDs) are used to determine the probability of having a glitch with duration D_k.

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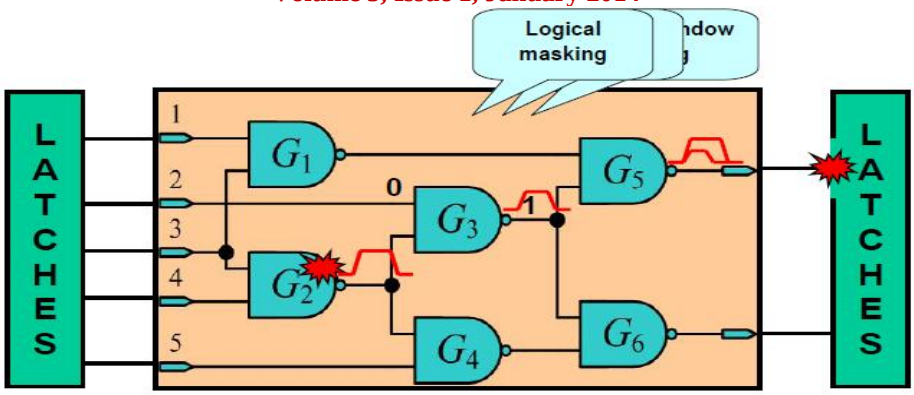

Fig. 1 Benchmark circuit (c17)

Algebraic decision diagram for above circuit,

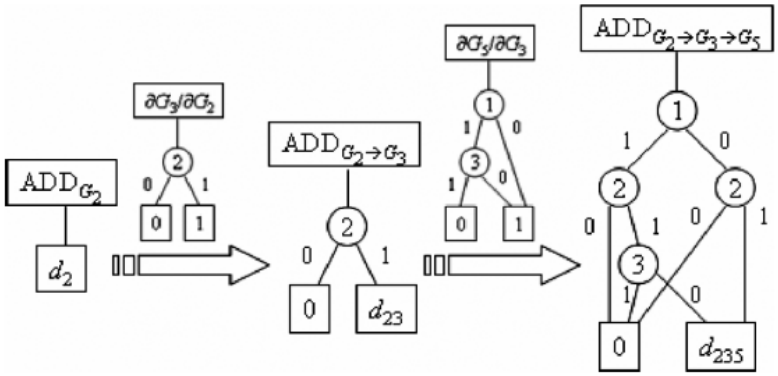

Fig. 2 Duration ADDs for a glitch originating at gate G_2 , and passing through gates G_3 and G_5 respectively

The ADD with terminal node "0" related with a gate represents all cases where a glitch is logically or electrically masked; the remaining values for duration or amplitude after a glitch passes through a gate that was represented by other terminal nodes. The glitch originating at that gate is obtained by built the initial ADD of every gate.

III. SER REDUCTION BY RAR METHODOLOGY

Using Redundancy Addition and Removal Iteratively add and remove redundant wires to minimize a circuit in terms of literal count. Accept only those with positive impact on SER. This method having benefits over other procedures because of very little area overhead, integrated treatment of three masking factors through decision diagrams, accurate approximation of SER impact of added and removed wires and introduce constraints to guide the RAR technique toward SER reduction. According to the mandatory assignments Candidate wires for addition can be identified and these assignments are made during automatic test pattern generation (ATPG). Keep wires/gates with high masking impact and to remove wires/gates with high error impact are the basic principle of our proposed framework. Mean masking impact (MMI) and mean error impact (MEI), used as key parameters for guiding the RAR-based approach.

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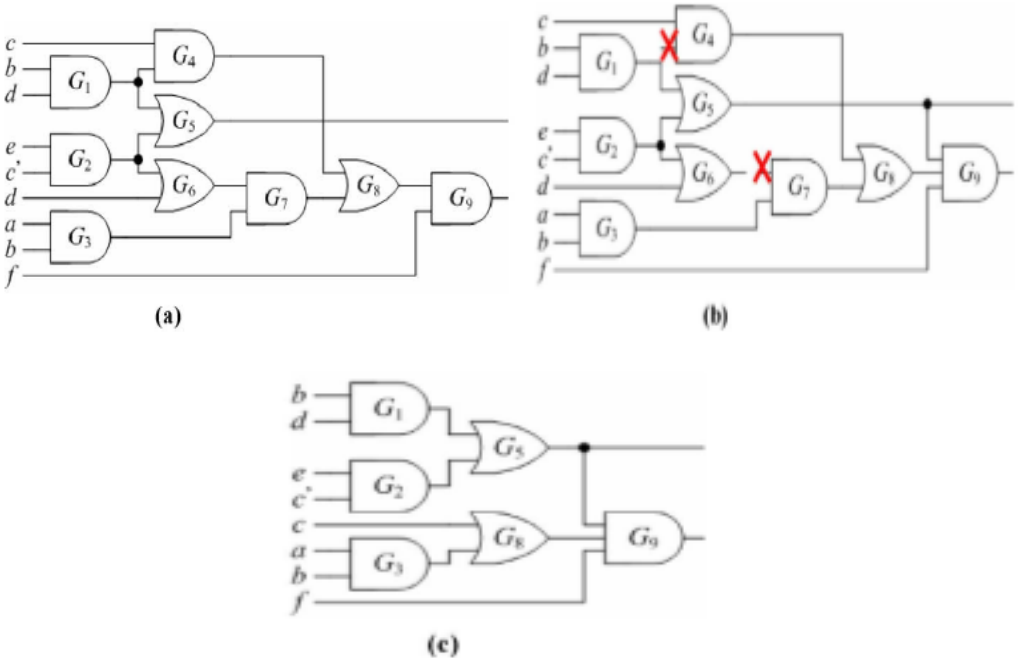

Fig. 3 Example of redundancy addition and removal (a) Original circuit. (b) The circuit after redundancy addition ($G_5 \rightarrow G_9$). (c) The circuit after redundancy removal ($G_1 \rightarrow G_4$) and ($G_6 \rightarrow G_7$)

In above example circuit he mandatory assignments for gate G_6 stuck-at-1 fault {f=1,G_3=1,G_4=0,G_6=0} from which we can get the implications{d=0, G_1=0,G_2=0,G_5=0}. If a wire from gate G_5 to gateG_9 is added into the circuit, there will be a conflicting assignment because gate G_5 should be set to "1" to make gate stuck-at-1 fault observable at outputs. So wire is a candidate for wire addition. One still needs to check if the candidate wire is indeed redundant; i.e., the wire does not change the circuit functionality. In Fig. 3 (b), wire G_5-G_9 is redundant. After adding wire G_5-G_9 into the circuit, wires G_1-G_4 and G_6-G_7 become redundant as compatible mandatory assignments do not exist for both of them. So they can be removed it is marked as 'X'. Fig.3(c) shows the resulting circuit after redundancy removal. The circuit becomes smaller if the removed redundancies are more than the added redundancies. For our objective of SER reduction, using redundancy addition and removal in an unsystematic manner may increase SER by reducing the number of gates or the depth of circuits.

A. Mean Error Impact: MEI quantifies the probability that at least one primary output is affected by a glitch originating at the gate. The larger MEI a gate has, the higher the probability that a glitch occurring at this gate will be latched.
Mean error impact (**MEI**) of each internal gate G_i is defined as,

$$\mathrm{MEI}\left(G_i^{d,a}\right) = \frac{\sum_{k=1}^{n_f}\sum_{j=1}^{n_F} p\left(F_j | G_i \text{ fails} \cap \text{init-glitch}=(d,a)\right)}{n_f \cdot n_F} \quad (2)$$

Where

n_F - cardinality of the set of primary outputs in the circuit{F_j}

n_f - cardinality of the set of probability distributions {f_k}

B. Mean Masking Impact: MMI denotes the normalized expected attenuation on the duration of all glitches passing through it. The larger MMI a gate has the more capable of masking glitches this gate is. Mean masking impact on duration (MMI) of each internal gateG_i,

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$$MMI_D(G_i^{d,a}) = \frac{\sum_{k=1}^{n_f}\sum_{j=1}^{n_G} MI_D(G_j^{d,a} \rightarrow G_i)}{n_G \cdot n_f \cdot d} \quad (3)$$

Where,

MI_D – Asking impact on duration of gate G_i

n_G – Cardinality of $C(G_i)$

$C(G_i)$ – Set of gates in the fan-in cone of gate G_i

C. Restrictions on RAR

1. Wire Addition Constraint

ΔMEI (*s*) = MEI (*t*) × [1-MMID (*t*)]

Wire *w* (*s*→ *t*) can be added only if

MEI (*t*) <*T*1

MMID (*t*) >*T*2

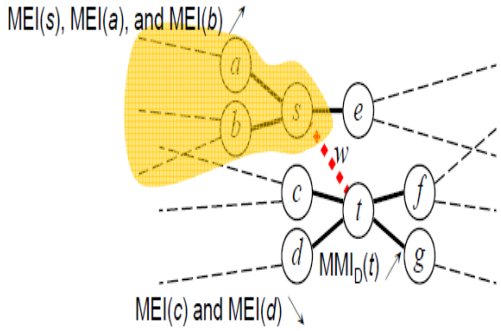

Fig. 4 Changes in MEI and MMI after adding wire w (s→ t)

2. Wire removal restriction

Wire *w*' (*u* →*v*) can be removed only if

- Wire *w*' is crucial in logical masking at gate *v*.
- The probability that gate *u* goes to the controlling value of gate *v* is sufficiently low.

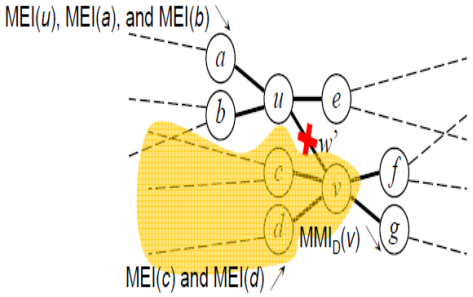

Fig. 5 Changes in MEI and MMI after removing wire w'(u→ v)

Benchmark circuit c432 that is 27-channel interrupt controller has been taken for framework. It consists five modules as M1, M2, M3, M4, and M5.The input channels are grouped into three 9-bit buses (we call them A, B and C), where the bit position within each bus determines the interrupt request priority. A fourth 9-bit input bus

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(called E) enables and disables interrupt requests within the respective bit positions. The seven outputs PA, PB, PC and Chan [3:0] specify which channels have acknowledged interrupt requests. Here module M4 consider for our framework.

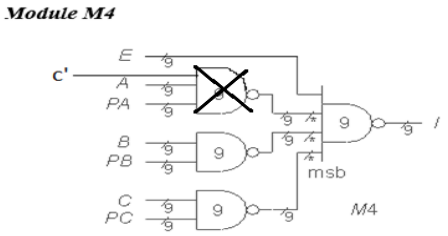

Fig. 5 Circuit with redundancy addition

Each NAND gate consists of the nine NAND gates in it. According to our RAR algorithm add the redundancy wire c' to the gate having fan-in inputs A& PA. Upon adding the redundancy wire c' the function of entire circuit will not change.

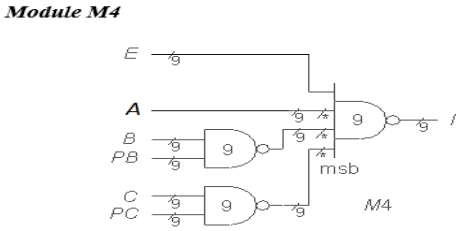

Fig.6 Circuit after redundancy removal

At the same time when that particular gate is removed, then the function of entire circuit will not change. So, gives the input 'A' can be given directly to the next gate. That is marked as 'X'.

IV. SIMULATION RESULTS

Fig.7 Simulation of original c432

Fig. 7 shows the output result of original benchmark circuit. This circuit consists of five modules. It has 36 inputs and 7 outputs with 162 gates without adding any redundancy wires.

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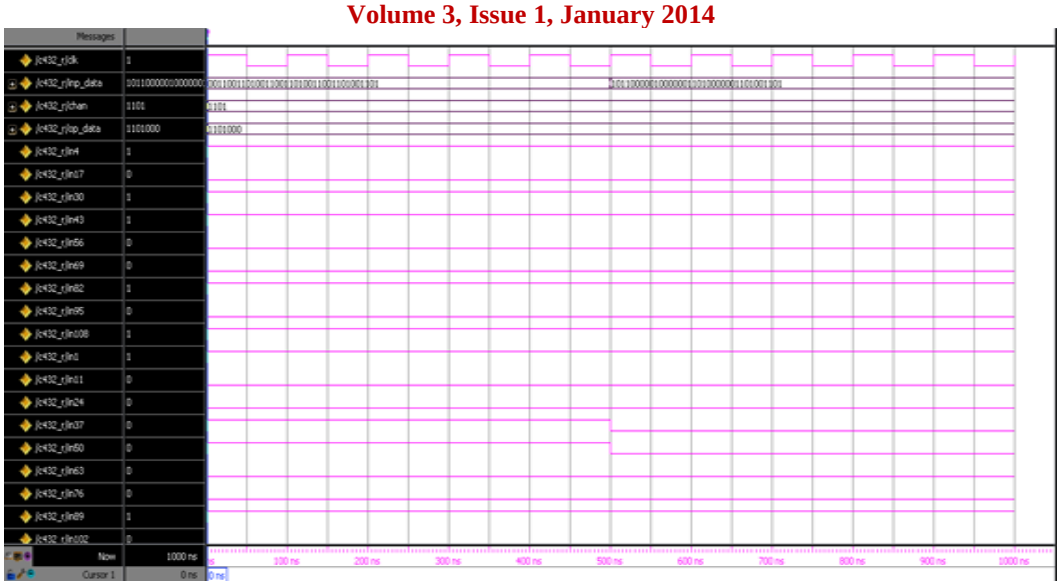

Fig. 8 Simulation for a after redundancy removal circuit

Fig. 8 Provides the result when add the redundancy wire c' to the gate with input A&PA then function of whole circuit will not change. Then while analyzing the operation of that particular gate if we remove that gate it would not affect the entire circuit operation.

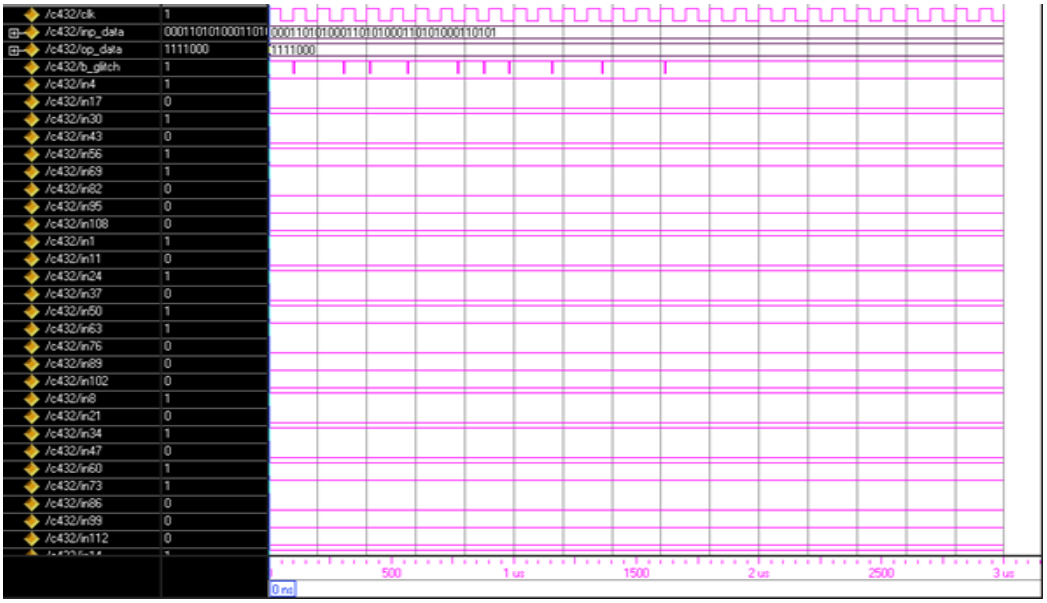

Fig.9 Original circuit with glitch

Fig. 9 depicts the output of the original circuit with glitches. In the original c432 circuit introduce some glitches in the module M4. In order to show the circuit performance with glitches after removal of that particular gate the simulation is presented.

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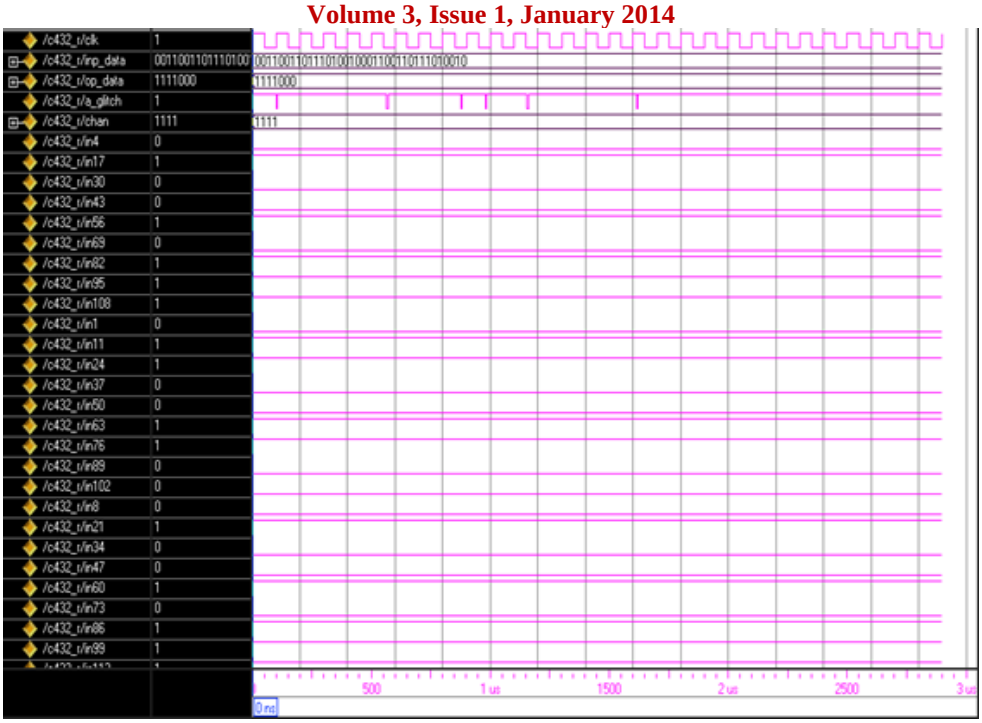

Fig.10 Optimized circuit with less glitch

Fig.10 shows the output of the optimized circuit with less glitch. In the original c432 circuit introduce some glitches in the module M4. In order to show the circuit performance with glitches after removal of that particular gate the simulation is presented.

Table I Comparison result of Benchmark circuit c432

METHOD	AREA OVERHEAD	POWER OVERHEAD (mw)	SER
ORIGINAL	162	71	10
OPTIMIZED	24	55	6

Table. I consists of the comparison results of original circuit and optimized circuit with Area overhead and power overhead and then corresponding soft error reduction. The above values obtained by when RAR approach used for c432 benchmark circuit that is 27-channel interrupt controller. Here the gate count is reduced from 162 to 24 implies the area overhead then Power overhead reduced from 71 to 55 mw. SER ranges from 10 to 6.

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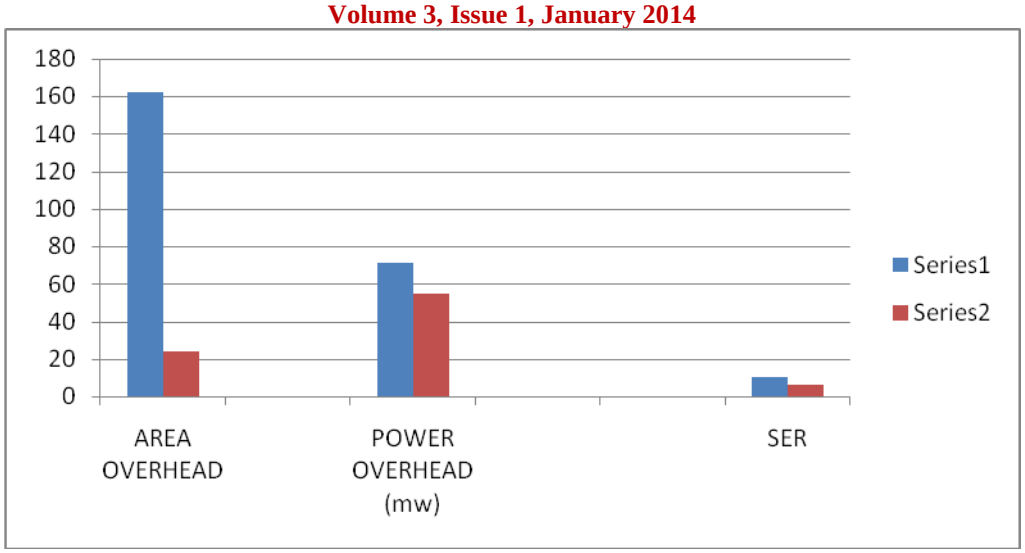

Fig.11 Overall analysis result of c432

V. CONCLUSION

Based on redundancy addition and removal method the proposed technique for soft error reduction is done by using symbolic SER analysis for combinational logic. SER reduction guided through two metrics (MEI and MMI) and three restrictions. Experiments on a separation of ISCAS'85 and MCNC'91 benchmarks expose the value of our procedure. This technique is easily applicable to sequential circuits in concurrence with an exact and efficient SER analyzer for sequential circuits.

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