A Novel Approach to Reduce Clock Power by Using Multi Bit Flip Flops

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Abstract- In modern VLSI designs, power consumed by clocking has taken a major part of the whole design. Reducing the power consumption not only can enhance battery life but also can avoid the overheating problem, which would increase the difficulty of packaging or cooling. As ICs become more complex, the problem of supplying accurate and synchronized clocks to all the circuits becomes increasingly difficult and also the power consumed by clocking becomes high. In order to reduce power consumption of clock signal an approach called multi bit flip flop has been introduced. It replaces several flip flops with multi bit flip flops which results in less number of clock signal and so less power consumption. Since the numbers of clocks are reduced it may affect the performance of the original circuit. To circumvent this problem without timing and placement capacity constraints violation, several techniques has been proposed. To identify the flip flops that can be merged and their legal regions co-ordinate transformation can be performed. To list out possible combinations of flip-flops provided by a library we build a combination table. Finally, merging of flip flops is done in hierarchal ways. Total wire length problem is also considered along with power reduction.

Index Terms- Reduction of clock power, replacing flip-flops, total wire length, merging.

I. INTRODUCTION

In latest years, the low power system has gained more importance because of the high requirement for portable electronic products. The numbers of components keep on increasing as technology enhances which leads to higher power density. Since the number of components increasing, dissipation of power is also increasing. This creates the necessity of power consumption reduction in order to improve the battery life and also evade overheating problem. Consequently, it has become a huge task for the designers to consider the power consumption in complex ICs. Moreover, power has become an important issue in modern VLSI design especially for those designs using deeply scaled CMOS technologies. Effective approaches have been projected to tackle this problem.

Here an efficient approach named Multi-Bit Flip-Flop has been introduced to reduce the clock power consumption in which some flip flops are replaced by smaller amount of multi bit flip flops. When flip flops are reduced in number obviously number of clock sinks are reduced in clock tree synthesis which would lead to smaller power consumption.
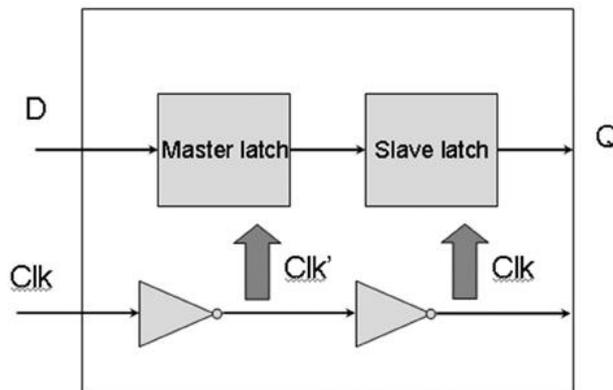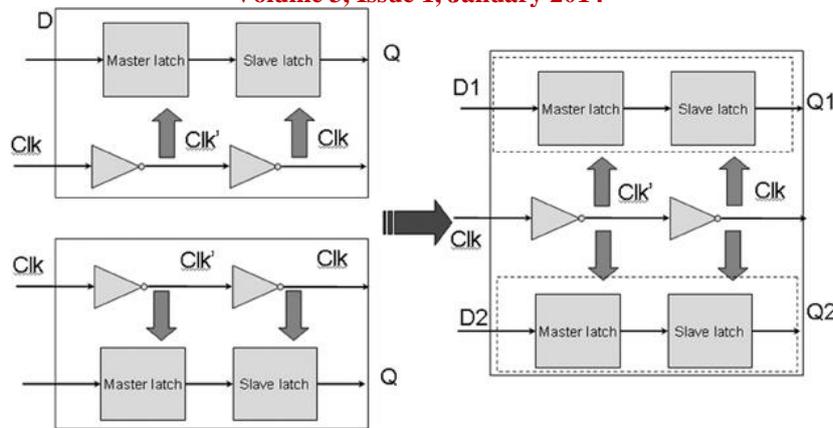

Fig. 1 Single bit flip-flop

Fig. 2 Merging two 1-bit flip-flops into one 2-bit flip-flop

Besides, device variations in the corresponding circuit can be reduced effectively when lesser flip flops are replaced by greater multi bit flip flops. Driving capability of the inverter based clock buffer increased expressively as CMOS technology advances. It indicates that several flip flops can share a common clock buffer to avoid wastage of power. Fig. 1 (a) shows the two 1-bit flip flops. Those flip flops are replaced by one 2-bit flip flop by sharing common clock buffer. It is shown in Fig. 1 (b). Since we perform replacement of flip flops, locations of some flip flops would be changed. It results in change in wire lengths of nets connecting pins to a flip-flop. The restriction of wire lengths of nets connecting pins to a flip-flop that cannot be longer than specified values after this process should be performed in order to avoid the violation of timing constraints. Area capacity of the region also considered here to assure that a new flip-flop can be placed within the preferred region. Two flip-flops of 1-bit are replaced by one flip-flop of 2-bit that is f1 and f2 are replaced by f3. It is shown in Fig. 2 (a). It results in change in wire lengths of nets net, net2, net3, and net4.After replacement, the Manhattan distance of new nets net1, net2, net3, and net4 cannot be longer than the specified values to avoid the timing violation. The entire placement region is divided into numerous bins, and each bin has an area capacity denoting the remaining area that extra cells can be placed within it. It is shown in Fig. 2 (b). Consider the area of $f3$ is 7. It is assigned to be placed in the same bin as $f1$. Since the remaining area of the bin is smaller than the area of $f3$, we cannot place $f3$ in that bin. It is also required to check the accessibility of new flip flops in the cell library. For example, when we wish to replace 2 and 3 bit flip-flops by a 5 bit flip-flop we have to check the availability of a 5 bit flip-flop in the cell library.

A. Background Work

As presented in [1] the basic idea is to reduce clock power and switching power by performing activity-based register clustering and activity-based net weighting respectively. In register clustering clock power is reduced by placing registers in the same leaf cluster of the clock trees in a smaller area. In net weighting, assignment of combination of activity and timing weights to the nets with higher switching rates or more critical timing reduces the switching power. In case of [2] they have used flip-flop clustering and placement algorithm in order to reduce flip-flop power consumption. Due to shared clock drivers and clock gating cells, smaller interconnecting wire length and design area is achieved. Since they are using common clock and enable signals for a group of flip-flops and reduced depth of a clock tree clock skew controllable. Due to fewer clock sinks and smaller capacitive load on the clock net less delay and power of the clock network is achieved. All these factors results in less power consumption of clock network. The key idea presented in [3] is to minimize the clock power compared to the conventional flip-flop with the help of leak current cut-off mechanism which is composed of a reduced clock swing driver and a special flip- flop. One of the reasons for this large power consumption of the clock system is that the transition probability of the clock is high. Since the power consumption of the clock system is proportional either to the clock swing or to the square of the clock swing, based on the circuit configuration, it is effective to decrease a clock voltage swing in order to reduce the clock system power.

II. IMPLEMENTATION OF ALGORITHM

This algorithm has three effective consecutive steps to handle the power reduction problem. In first step transformation of coordinate system of cells is performed in order to identify what are the flip-flops can be

merged. Building a combination table is done in the second step which avoids the wasting of time in finding impossible combination of flip-flops. In the third step of flip-flop replacement, in order to reduce the complexity whole chip region is partitioned into several subregions then flip-flop replacement is performed. Fig. 3 depicts this flow.
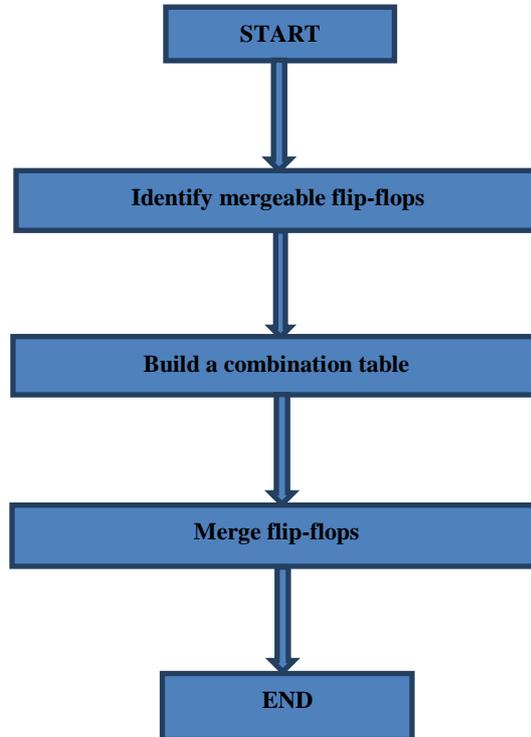

Fig. 3 Flow of algorithm

A. Transform the placement space

At first, based on timing complexity on different pins associated with flip-flop feasible placement region is identified. Overlapping of feasible placement regions helps to find legal placement region f_i. But the problem with the overlapped region is that it is diamond in shape which complicates identification of overlapped region. The solution is to change the overlapped region into rectangular region by using transformation of coordinate cells.
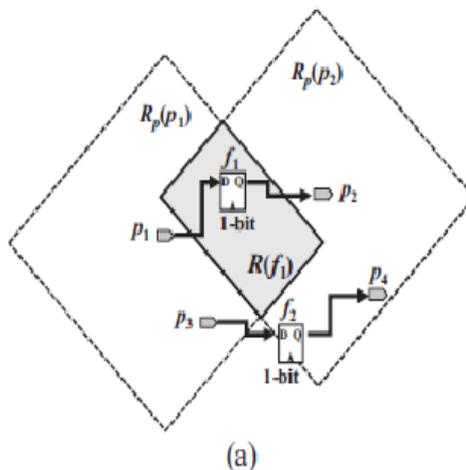

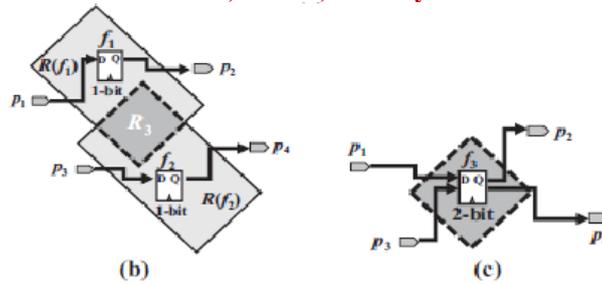**Fig. 4 (a) Feasible placement regions $R_p(p_1)$ and $R_p(p_2)$ obtained for pins p_1 and p_2**

Fig. 4 (b) Legal placement regions $R(f_1)$ and $R(f_2)$ obtained for f_1 and f_2

(c) New flip-flop f_3 which replaces f_1 and f_2

A flip-flop f_1 with its two pins and its feasible regions is depicted in fig. 4 (a). The pins are represented by p_1 and p_2. Feasible placement regions of p_1 and p_2 are shown in spotted lines and it is given by $R_p(p_1)$ and $R_p(p_2)$ respectively. $R(f_1)$ and $R(f_2)$ respectively. Legal placement region for a flip-flop f_1 is overlapping of feasible placement regions which is represented by $R(f_1)$. From the Fig. 4 (b) we conclude that the replacement of f_1 and f_2 by f_3 is possible since their feasible placement regions are getting overlapped. New flip-flop f_3 is presented in Fig. 4 (c).
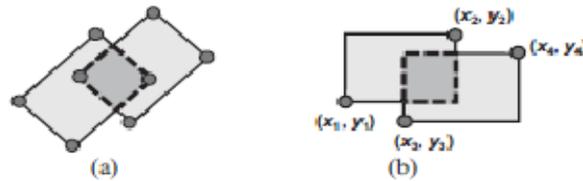

Fig. 5 (a) Diamond shape obtained by Overlapping of two legal regions
(b) Changing of diamond shape into Rectangular shape by $45°$ rotation of (a)

To store this overlapped region we need four coordinates since it has diamond shape. This is depicted in Fig. 5 (a). Rotation of $45°$ at each segment converts the diamond region into rectangular region which needs only two coordinates to store and this makes identification of overlapped region simple. It is represented in Fig. 5 (b). The diamond region before transformation and rectangular region after transformation is shown as spotted lines.
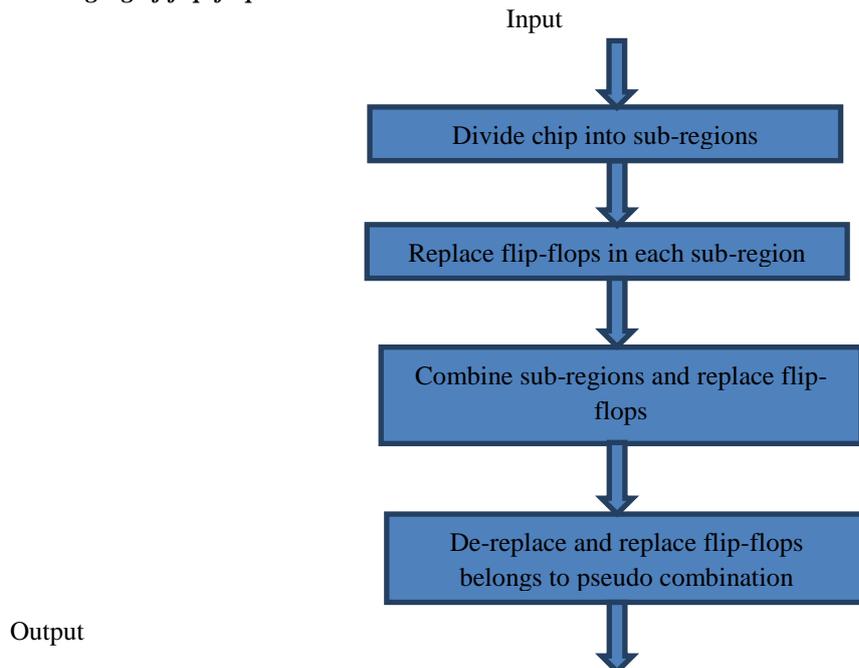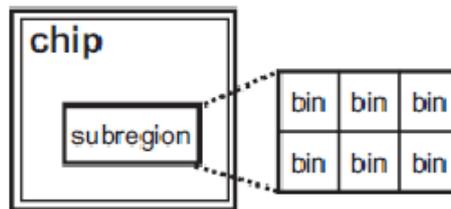
B. Merging of flip-flops

Fig. 6 Flow for merging flip-flops

Before merging flip-flops a combination table is built which includes all possible combinations of flip-flops. Flip-flops in the combination table should be feasible. By using this combination table flip-flop merging is being performed. For the purpose of complexity reduction, entire placement region is partitioned into several subregions. Combination all subregions results in total placement region. In each subregion flip-flop replacement is performed and since smaller regions forms larger regions flip-flop replacement in neighbouring regions also possible. Fig. 6 shows the flip-flop replacement flow.

1. Partitioning and replacement of placement region and flip-flops

Fig. 7 shows the partitioned region with several subregions each subregion having six boxes or bins. By selecting accurate partition method reduction of computational complexity can be achieved. The aim of partitioning is to increase the speed of the problem.


Fig. 7 Partitioning of placement region

Replacement of flip-flops is carried out based on the combination table that we built earlier. At first flip-flop types under the combinations already present in library are linked. Here we represent combination table as T and flip-flop combinations as n. For each and every combination n mentioned in combination table, merging of flip-flops is performed depend upon the link from leaves to root i.e flip-flops under left child and right child of n. Binary tree is used to find the flip-flop combination arranged with left and right child. Flip-flops under left child is called l_{left} and right child is l_{right}. Depending upon the acceptable cost, f_{best} the best flip-flop present in l_{right} is selected in order to merge it with the f_i in l_{left}. It continued for all flip-flops in l_{left}. If the two flip-flops are merged with an acceptable cost then the combination cost is calculated for that pair. At the last we replace all selected flip-flops with a fresh flip-flop.

2. Bottom-up flow for combinations of subregions

A new flip-flop can swap two flip-flops in similar subregion. There are possibilities to merge flip-flop with a flip-flop in nearby regions. In order to save power some subregions are united together to make giant subregion and flip-flop replacement is performed in new bigger subregion. We can stop replacing flip-flops if there is no more giant subregion exists.
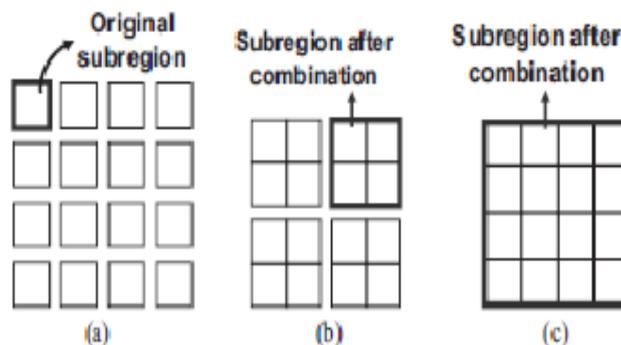
Fig. 8 Combining subregions into a giant region

Fig. 8 (a) shows the total placement region with sixteen subregions. Replacement of flip-flops is executed in each subregion and then giant subregion is formed by uniting few subregions. Here, combination of four subregions leads giant subregion. It is depicted in Fig. 8 (b). If there are flip-flops still waiting to be merged with neighbouring subregions all the subregions in Fig. 8 (b) is merged together and forms total region and replacement should be executed in entire region. This is depicted in Fig. 8 (c).

III. EXPERIMENTAL RESULTS

Three benchmark circuits ISCAS298, ISCAS208 and ISCAS5378 were selected and the concept explained above was implemented in those circuits. All the three circuits consist of D type flip-flops. The simulation results were taken by using Xilinx and Modelsim software tools.

Fig. 9 represents the output waveform for the Benchmark circuit ISCAS298. It has four flip-flop groups 6, 4, 2 and 2. The pseudo types are created as 1, 5, 4, 2 and 2 and then they are sorted as 1, 2, 2, 4 and 5. The delay values for each kind of flip-flop group are found. Here first three flip-flop groups are not violating threshold value hence they are merged together. Since fourth and fifth groups are violating threshold value they are not merged and individual clock is given to those flip-flops.

Fig. 10 represents the output waveform for the Benchmark circuit ISCAS208. It has three flip-flop groups 1, 2 and 5. The pseudo types are created as 1, 2, 3 and 2 and then they are sorted as 1, 2, 2 and 3. The delay values for each kind of flip-flop group are found. Since no flip-flop group is violating threshold value, all flip-flops are merged together.
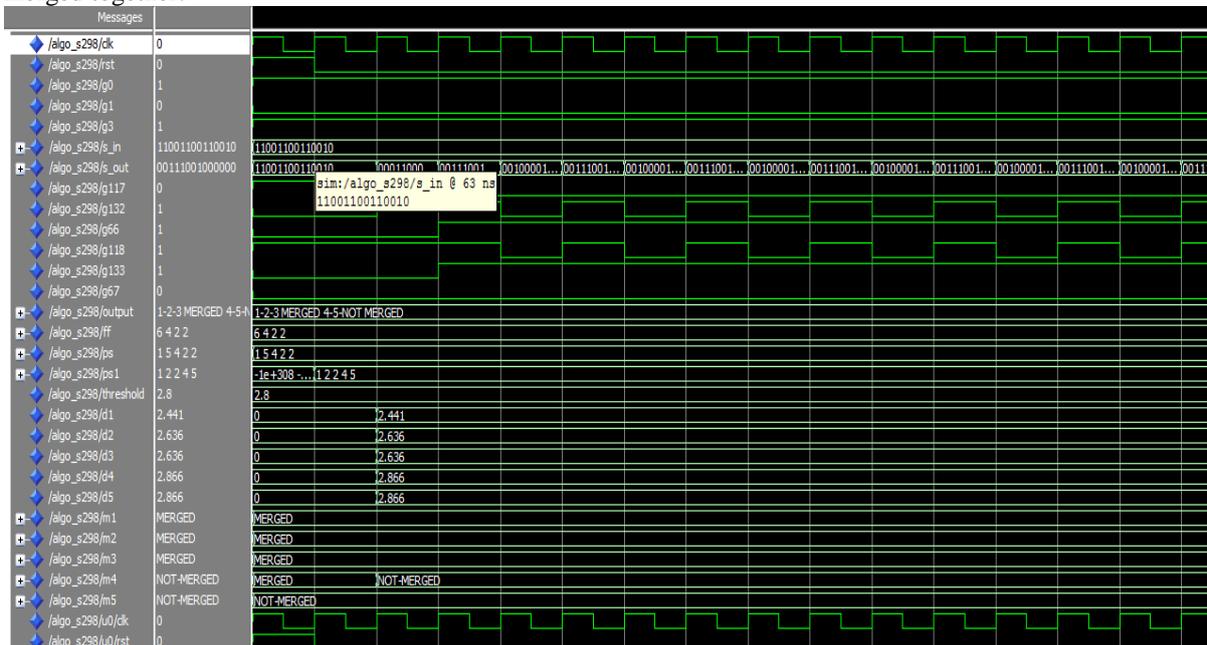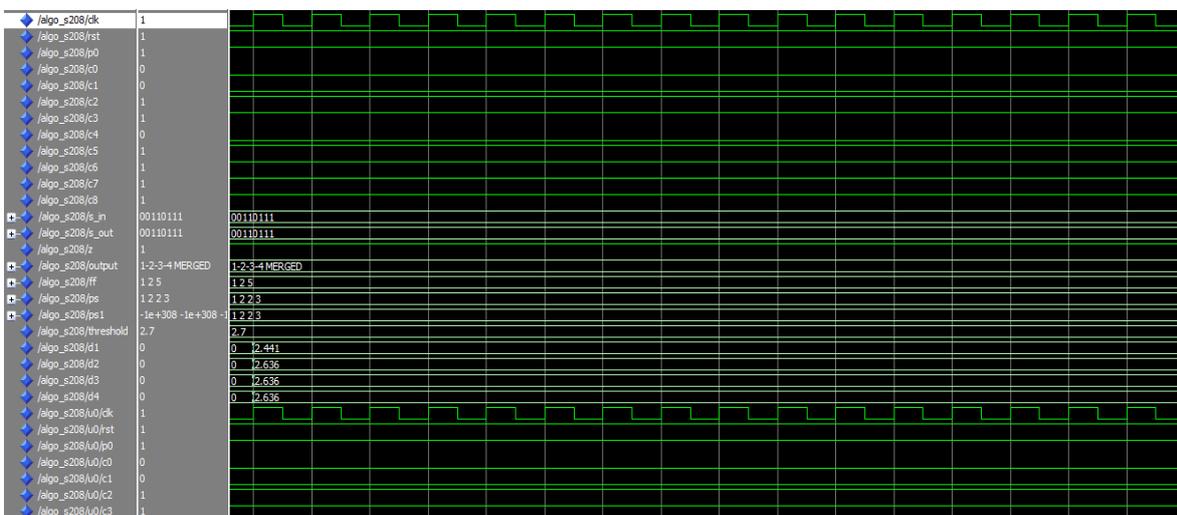

Fig. 9 Output of ISCAS298 benchmark circuit

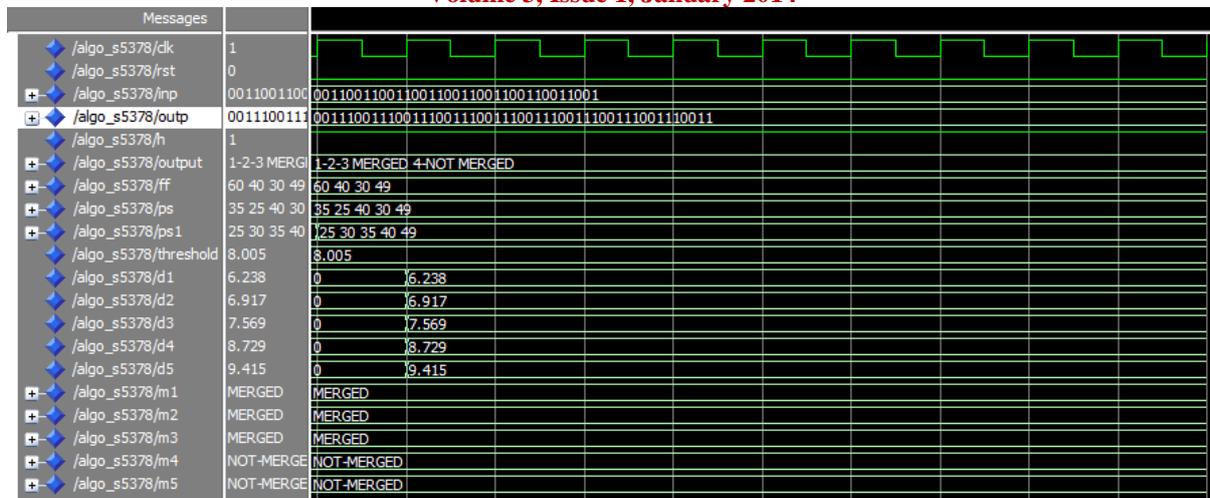**Fig. 10 Output of ISCAS298 benchmark circuit**

Fig. 11 Output of ISCAS298 benchmark circuit

Fig. 11 represents the output waveform for the Benchmark circuit ISCAS298. It has four flip-flop groups 6o, 40, 30 and 49. The pseudo types are created as 35, 25, 40, 30 and 49 and then they are sorted as 25, 30, 35, 40 and 49. The delay values for each kind of flip-flop group are found. Here first three flip-flop groups are not violating threshold value hence they are merged together. Since fourth and fifth groups are violating threshold value they are not merged and individual clock is given to those flip-flops. Table. I represents the power and area comparison for the benchmark circuits ISCAS298, ISCAS208, ISCAS5378 before and after merging flip-flops. Before merging it was high and after merging it got reduced. The power is expressed in terms of mill watt and the area is expressed in terms of gate counts. For S298 it gives 51.23% reduction in power and 42.85% in area. For S208 it gives 51.28% reduction in power and 50% in area. For S5378 it gives 51.16% reduction in power and 43.74% in area.

Table. I Performance analysis for S298, S208, S5378

S298

Parameters	Number of individual clock	Power(mw)	Area(Gate count)
Before merging	14	162	112
After merging	9	79	64

S208

Parameters	Number of individual clock	Power(mw)	Area(Gate count)
Before merging	8	78	64
After merging	0	38	32

S5378

Parameters	Number of individual clock	Power(mw)	Area(Gate count)
Before merging	179	1497	1294
After merging	89		728

The power reduction ratio can be defined as the ratio of difference between original power and merged power to the original power.

$$PR\_RATIO(\%) = \frac{power_{original} - power_{merged}}{power_{original}} \cdot 100\%$$

The wire length reduction ratio can be defined as the ratio of wire length after merging to the original wire length.

$$WR\_RATIO(\%) = \frac{wirelength_{merged}}{wirelength_{original}} \cdot 100\%$$

Table. II Power and Wire length Reduction Ratio for S298, S208, S5378

Benchmark circuits	PR_Ratio	WR_Ratio
ISCAS298	51.23	57.14
ISCAS208	51.28	50
ISCAS5378	51.16	56.25

Table. II represents the power and wire length reduction ratio for three Benchmark circuits ISCAS298, ISCAS208, and ISCAS5378. It has been calculated by using corresponding formulas given above. This algorithm reduces power and area not only for D type flip-flop. It works for different types of flip-flops. Here we have replaced D flip-flop with an Edge Triggered Latch (ETL) flip-flop and worked out the same procedure and measured power and area using same tools. ETL flip-flop is shown in Fig. 12. Performance analysis for ETL flip-flop is given below.
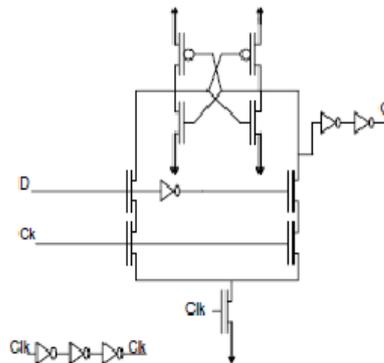

Fig. 12 New ETL flip-flop

Table. III Performance analysis for S298, S208, S5378 with ETL flip-flop
S298

Parameters	Number of individual clock	Power(mw)	Area(Gate count)
Before merging	14	81	168
After merging	9	66	84

S208

Parameters	Number of individual clock	Power(mw)	Area(Gate count)
Before merging	8	54	96
After merging	0	36	48

S5378

Parameters	Number of individual clock	Power(mw)	Area(Gate count)
Before merging	179	1090	1782
After merging	89	652	859

Table. III represents the power and comparison for the benchmark circuits ISCAS298, ISCAS208, ISCAS5378 before and after merging flip-flops. Before merging it was high and after merging it got reduced. For S298 it gives 18.51% reduction in power and 50% reduction in area. For S208 it gives 33.34% reduction in power and 50% reduction in area. For S5378 it gives 40.18% reduction in power and 51.79% reduction in area.

Table. IV. Power and Wire length Reduction Ratio for S298, S208, S5378 with ETL flip-flop

Benchmark circuits	PR_Ratio	WR_Ratio
ISCAS298	18.51	50
ISCAS208	33.34	50
ISCAS5378	40.18	48.20

Table. IV represents the power ratio for three benchmark circuits ISCAS298, ISCAS208, and ISCAS5378. Ithas calculated by using corresponding formulas given above.
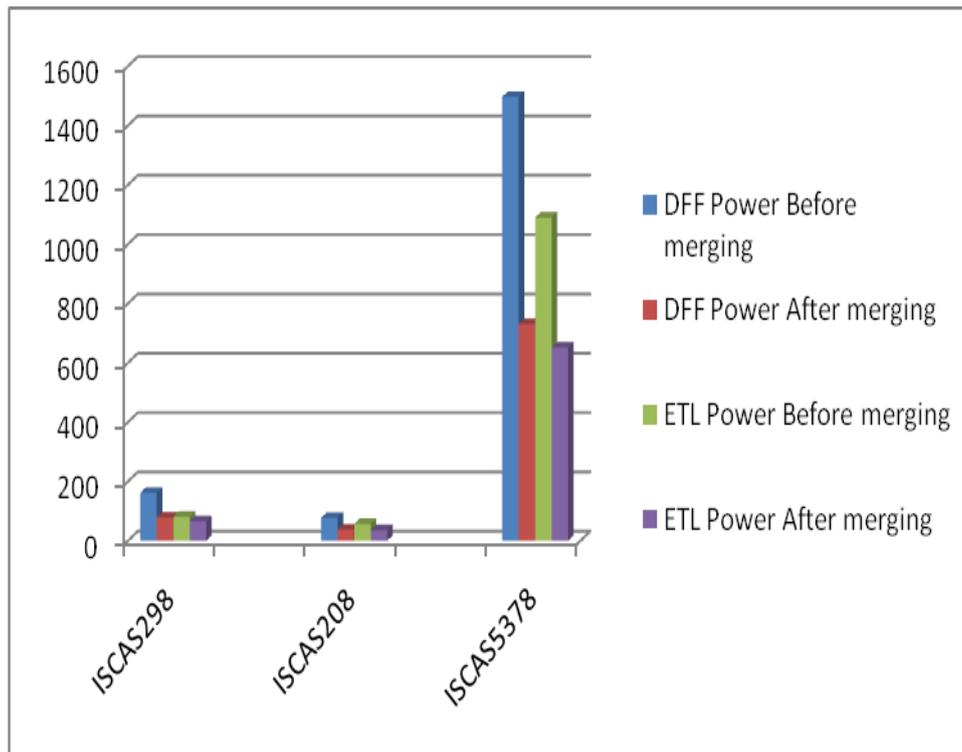

Fig. 13 Power analysis

Fig. 13 represents the power analysis for three benchmark circuits ISCAS298, ISCAS208, and ISCAS5378 before and after merging for both D flip-flop and ETL flip-flop. From the figure it is clear that for each circuit the power is high before merging flip-flops and it got reduced after merging flip-flops.
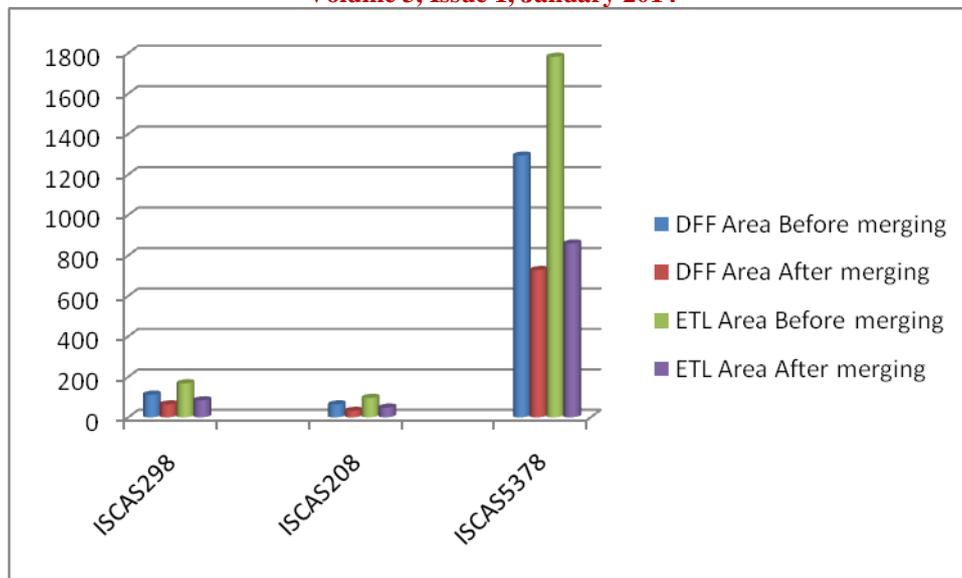
Fig. 14 Area analysis

Fig. 14 represents the area analysis for three benchmark circuits ISCAS298, ISCAS208, and ISCAS5378 before and after merging for both D flip-flop and ETL flip-flop. From the figure it is clear that for each circuit the area is high before merging flip-flops and it got reduced after merging flip-flops.

IV. CONCLUSION

For solving today's most important problem of power consumption in VLSI industry, an algorithm called flip-flop replacement has introduced here. This algorithm has three effective consecutive steps to handle the power reduction problem. In first step transformation of coordinate system of cells is performed in order to identify what are the flip-flops can be merged. Building a combination table is done in the second step which avoids the wasting of time in finding impossible combination of flip-flops. In the third step of flip-flop replacement, in order to reduce the complexity whole chip region is partitioned into several subregions then flip-flop replacement is performed. Along with power reduction wire length reduction problem also considered here.

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