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GLITCH Free NAND-based DCDL using dual Triggered Flip-Flop

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Abstract*— Digitally controlled delay line is a digital circuit used to provide the desired delays. Glitches are the most considerable factor that limits the use of DCDL in many applications such as DLL and clock generators. The NAND-Based circuit eliminates the glitches. This circuit uses control bits which can be generated by using dual triggered flip-flop. This flip-flop consumes more power. In the proposed method, power consumption is reduced by using dual edge triggered sense amplifier flip-flop.

***Index Terms*— All-digital delay-locked loop (ADDLL), Phase-locked loop (PLL), delay-line, flip-flops, sense amplifier, Dual edge triggered sense amplifier flip-flop (DET-SAFF).**

I. INTRODUCTION

Digital circuits are easy to handle compared to analog circuits and also digital circuits requires low power. Time-domain resolution of a digital signal is superior to voltage resolution of analog signals. DCDL is most important factor in the applications like PLL, ADDLL and ultra wideband receivers. DCDL has coarse and fine delay adjustments. The coarse delay is implemented as a mirror delay line. The fine delay can be implemented by cell library using available cells. In [1], for a CMOS digital DLL, the suitable conventional delay line uses inverters which provide the shortest delays. Although this is attractive, its limitations are coarse phase resolution and finite phase range. To overcome this, the complementary delay line is used. The "classical" approach [2], [3] to design a DCDL is using a delay-cells chain and a MUX to select the desired cell output. In these mux-based DCDLs, if the number of cells increases then the MUX delay also increases. To obtain the good linearity and resolution the delay elements are constructed by using NAND gates. The DCDL proposed in [9] is based on a cascade of equal delay elements. If each delay element is constructed by using an inverter and an inverting multiplexer simple layout is obtained. The paper is organised as follows. Glitch free DCDL is described in section-II. Driving circuits for control bits generations are described in section-III. Section –IV gives the conclusion of this work.

II. GLITCH FREE DCDL

A. DCDL WITH GLITCHES

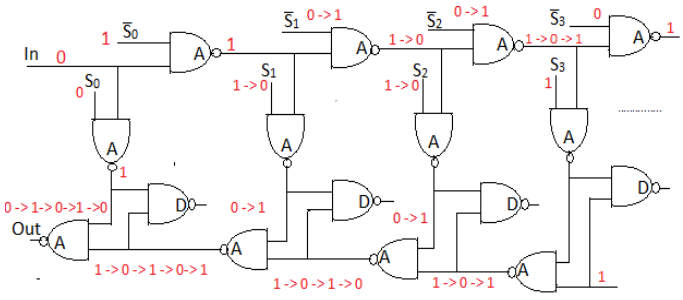

Fig 1.Diagram for Glitching problem in DCDL with glitches

In the NAND-based DCDL [5],[6], the delay element is constructed by using four NAND gates. This is shown in figure 1. In this figure "A" denotes the fast input of each NAND gate D represents the dummy cell used for load balancing. Here delay of the circuit is controlled by the control bit S_i. When S_i=0 the circuit is in pass state. If S_i=1 it is in turn state.

In DCDL applications, to avoid DCDL output glitching, the switching of delay control-bits is synchronized with the switching of *In* input signal. If the control-bits arrival time is lower than the arrival time of the input Signal, glitching is avoided. But in the DCDL of Fig. 1 this condition is not sufficient to avoid glitching. In this

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circuit, in fact, it is possible to have output glitches also considering only the control-bits switching, with a stable input signal. Let us name S= [S_0, S_1...] the vector of the control-bits of the DCDL. Let *In=0* and the control code c is switched from 1 to 2 resulting in glitches. If the control code is switched from 1 to 3, glitching is high. No glitching can occur when the control-code is decreased. When the control-code is increased by one, the glitching problem could be avoided by delaying S_i signals with respect to $\overline{S}_i$ signals. Figure 2 shows the simulation result using modelsim.

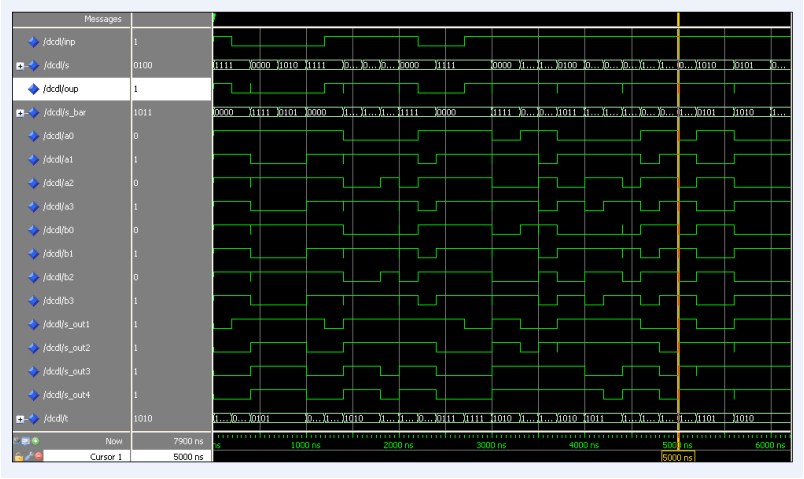

Fig 2. Simulation result of DCDL glitching

B. DCDL WITHOUT GLITCHES

Glitches in figure 1 are reduced by using two control bits S_i and T_i. Glitch free circuit (inverting) is shown in figure 3.

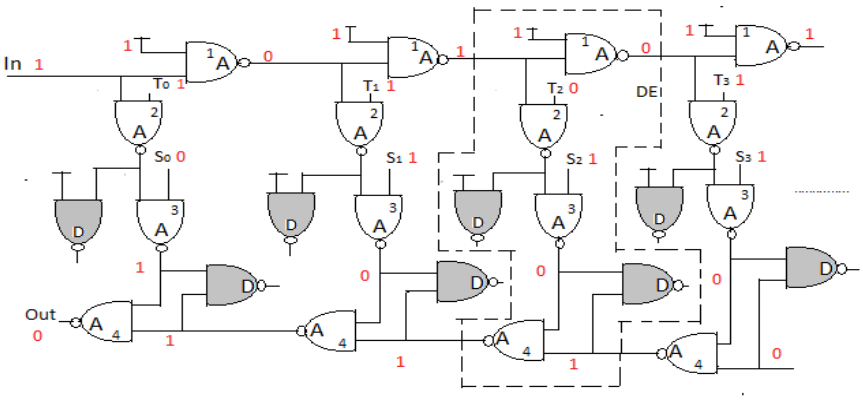

Fig 3.Glitch free NAND-Based DCDL (inverting)

In this figure "A" denotes the fast input of each NAND gate. Gates marked with "D" represents dummy cells added for load balancing. The different logic states are shown in table 1. When S_i=0 and T_i=1 the NAND "3" output is equal to 1 and the NAND "4" allows the signal propagation in the lower NAND gates chain. And if S_i=1 and T_i=1, the state is turn state. In this state the upper input of the DE is passed to the output of NAND "3". If S_i=1 and T_i=0 the state is post-turn state. In this DE the output of the NAND "4" is stuck-at 1, by allowing the propagation, in the previous DE (which is in turn-state), of the output of NAND "3" through NAND "4". The circuit of Figure. 3 is an inverting DCDL. In this circuit the first DE is never in post-turn state, therefore T_0 is always 1.

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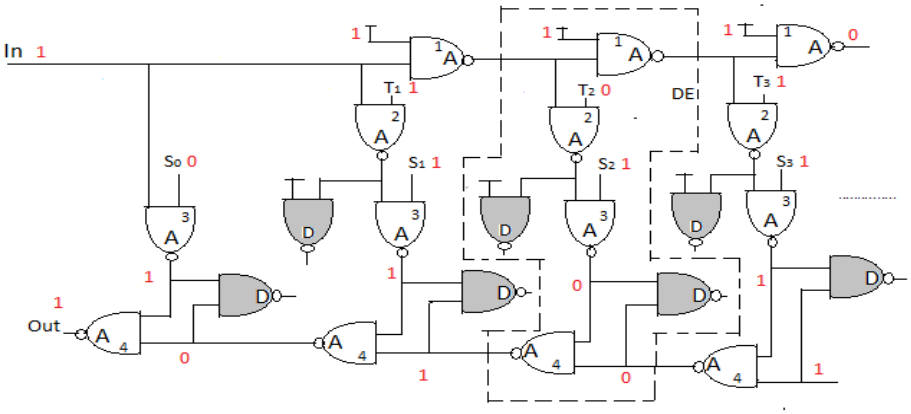

Fig 4.Glitch free NAND-Based DCDL (non-inverting)

TABLE I. LOGIC STATES OF EACH DE IN DCDL

T_i	S_i	DE State
1	0	Pass
1	1	Turn
0	1	Pass-Turn

The non-inverting DCDL is constructed by modifying only the first DE, as shown in Fig. 4. Here the NAND gates "1" and "2" of the first DE have been deleted, together with signal T_0. The signal a_1 of the second DE is now equal to In, therefore the behaviour of the DCDL is non-inverting. The non-inverting DCDL of Fig.4, therefore, maintains the same performances of the NAND-based DCDL of [4]–[6], while avoiding its glitching problem. The simulation result for inverting and non-inverting glitch free DCDL is shown in figure 5 & 6.

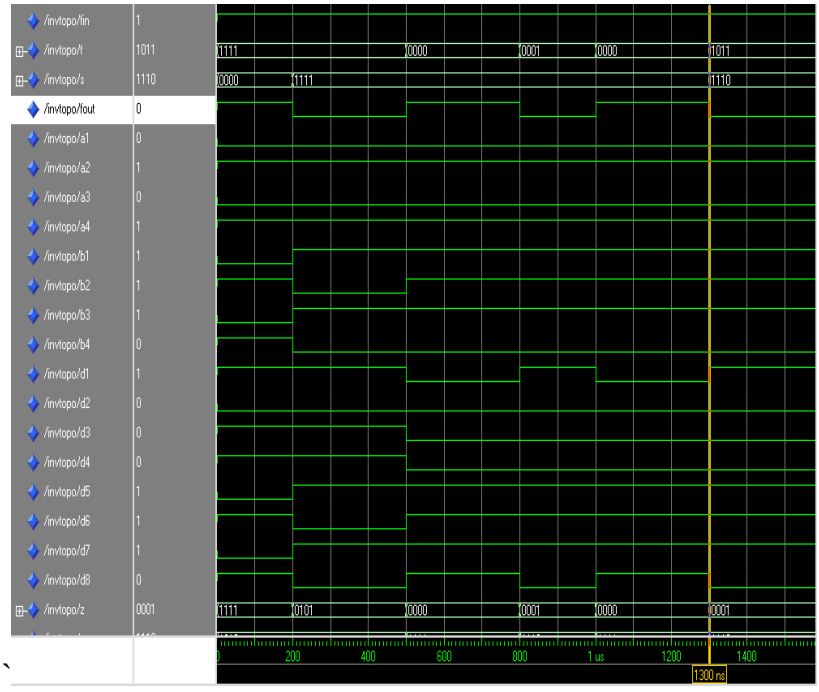

Fig 5.Simulation result of inverting glitch free DCDL

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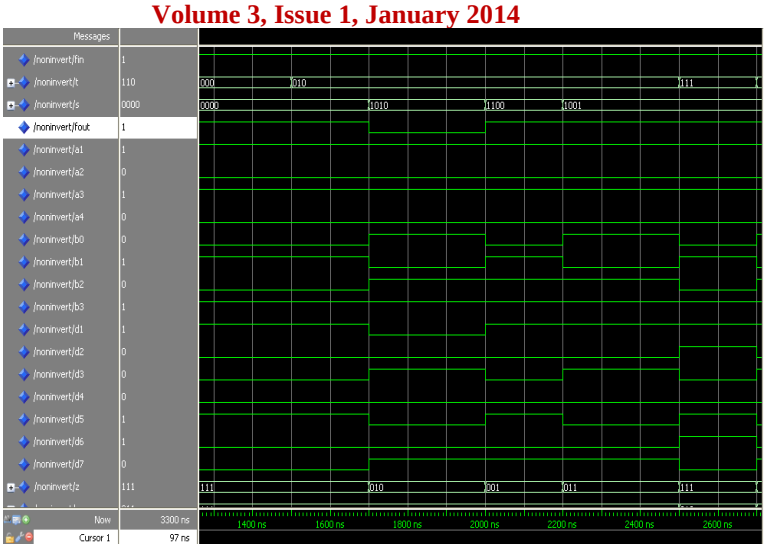

Fig 6.Simulation result of non-inverting glitch free DCDL

III. DRIVING CIRCUIT

Control bits are generated by using driving circuits. In [7] the possible driving circuits were analysed. It is concluded that dual triggered flip-flop is the best driving circuit shown in figure 7.

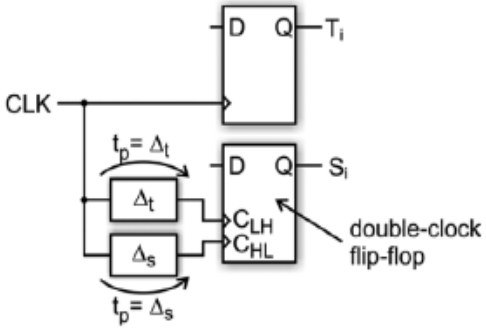

Fig 7.Double clock flip-flop: Si delayed with different LH/HL delays by using clock-tree delay and double-clock flip-flops

The dual triggered flip-flop based on sense amplifier topology is described in [7]. The circuit diagram is shown in figure 8. This is based on the sense amplifier based topology. The simulation result is shown in figure 9.

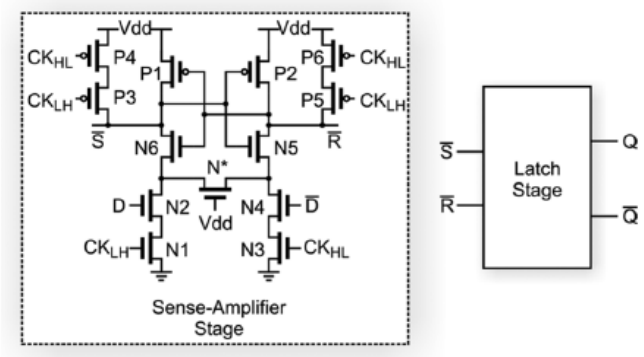

Fig.8.Existing Dual triggered flip-flop realized by using a sense-amplifier-based Topology

The simulation result is obtained using 250µm CMOS technology. Power is analysed using Microwind tool.

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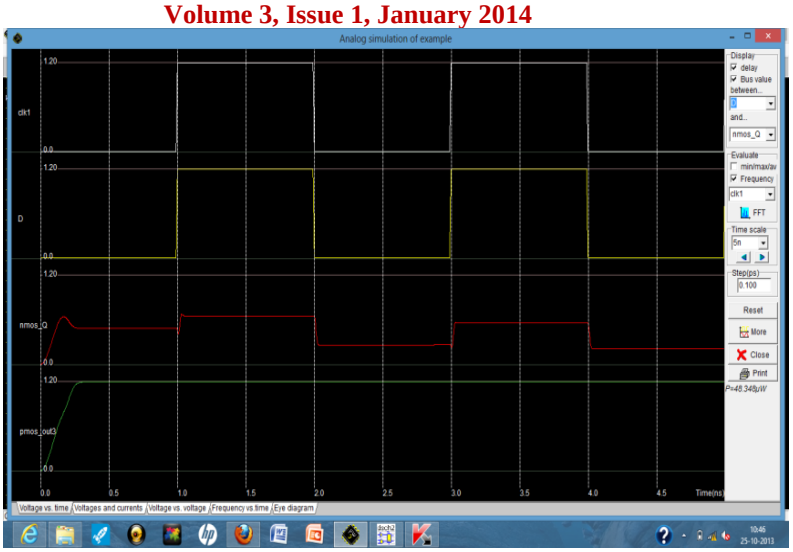

Fig 9. Simulation result of Dual triggered flip-flop realized by using a sense-amplifier-based Topology

A. DISADVANTAGE OF EXISTING DRIVING CIRCUIT CALLED DUAL EDGE TRIGGERED FLIP-FLOP

The dual triggered flip-flop based on sense amplifier driving circuit has more advantage than the driving circuit I and II in [7]. But the drawback is power consumption is high that is 48.345 Micro watts. This can be avoided by using the proposed Driving circuit.

B. PROPOSED DRIVING CIRCUIT

PROPOSED DUAL EDGE TRIGGERED SENSE AMPLIFIER FLIP-FLOP FOR CONTROL BITS GENERATION:

The schematic diagram of the proposed Dual Edge Triggered Sense Amplifier Flipflop is given in Fig.10. It consists of three stages: the pulse generating, sensing and the latching stage. At the rising and falling clock edges, dual edge triggered pulse generator produces a brief pulse signal. For a sense amplifier based flip-flop, in the evaluation phase, when D is low, SB will be set to high and when D value is high, RB will be set to high. So, in the sensing stage, the conditional pre charging technique is applied to avoid the redundant transitions at major internal nodes.

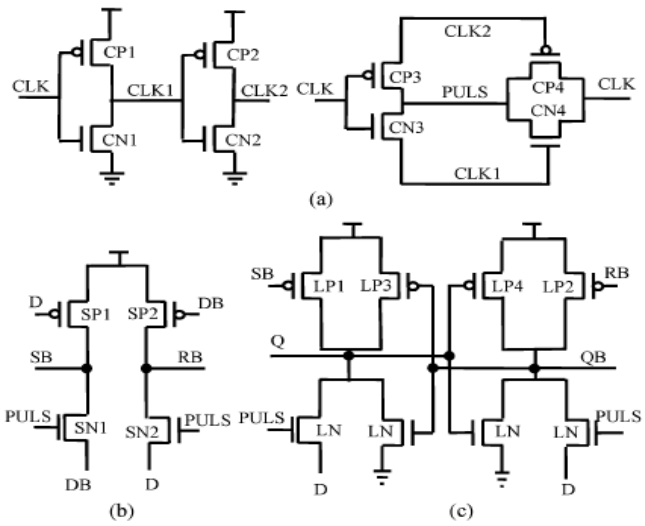

Fig 10.Proposed dual edge triggered sense amplifier flip-flop. (a) Dual pulse generator, (b) Sensing stage, (c) Symmetric latch

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In the pre charge paths of nodes SB and RB, two input controlled pMOS transistors, SP1 and SP2, are embedded. Here, if D remains high for n cycles, in the first cycle SB discharging may takes place. For the following cycles, SB will be floating when PULS is low or fed to the low state DB when PULS is high. RB needs to be pre-charged in the first cycle and remains at its high state for the remaining cycles. The critical pull down path of SB and RB is simplified since the pre-charging activity is conditionally controlled. This is used to reduce the discharging time. Therefore, the resulting sensing stage has low-power and high-speed features.

For further improvement in the operating speed, a fast symmetric latch is developed. The new latch makes use of SB and RB to pull up the output nodes. But the pull down path is modified. PULS-controlled nMOS pass transistor is composed by pull down path through which D (DB) is directly fed to the Q (QB) node. So high-to-low output transition getting speed because the output latch immediately captures the input value once the PULS signal is generated. On the other side, the low-to-high latency will also be improved. Pass transistors charges the output node with pull-up transistors, LP1 and LP2. Note that the pass transistors cannot fully charge a node to high, but it can assist with the pull-up transition. When the flip-flop is opaque, the output state is maintained by the transistors, LP3, LP4, LN3, and LN4. The simulation result is shown in figure 11. The power consumption of this circuit is 18.576µw. This is less compared to the existing driving circuit.

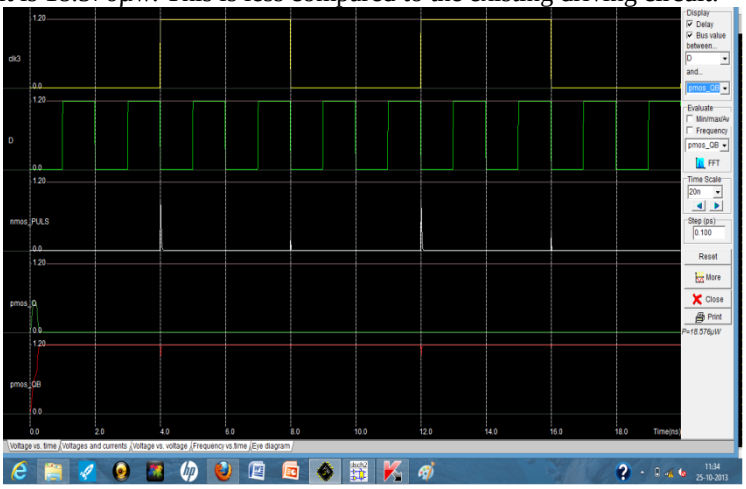
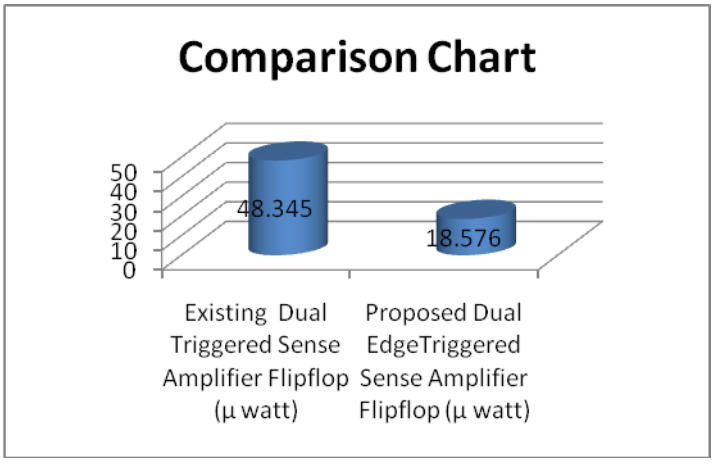


Fig 11.Simulation result of proposed dual edge triggered sense amplifier flip-flop



IV. CONCLUSION

A Digitally Controlled Delay Lines plays an important role in many applications. Glitches are the drawback of this DCDL.A NAND-based DCDL which avoids the glitching problem has been presented. Control bits are used to control the Digitally Controlled Delay Line circuit. And the power consumption of driving circuit is reduced by using the dual edge triggered sense amplifier flip-flop. The simulation results confirm the correctness of developed model and show that proposed solutions improve the resolution with respect to previous approaches.

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REFERENCES

[1] B.W. Garlepp, K.S. Donnelly, Jun Kim, P.S. Chau, J.L.Zerbe, Charless Huang, C.V. Tran, C.L.Portmann, Donald Stark, Yin-Fai Chan, T.H.Lee and M.A. Horowitz, "A Portable Digital DLL for High-Speed CMOS Interface Circuits," JSSC, 34(5):632-644, May 1999.

[2] B. M. Moon, Y. J. Park, and D. K. Jeong, "Monotonic wide-range Digitally controlled oscillator compensated for supply voltage variation", IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 55, no. 10, pp.1036–1040, Oct 2008.

[3] T. M. Matano, Y.Takai, T.Takahashi, Y.Sakito, I.Fujii, Y.Takaishi, H.Fujisawa, S.Kubouchi, S.Narui, K.Arai, M.Morino, M.Nakamura, S.Miyatake, T.Sekiguchi and K.Koyama, " A 1-Gb/s/pin 512-Mb DDRII SDRAM using a digital DLL and a slew-rate-controlled output buffer", IEEE J. Solid-State Circuits, vol. 38, no. 5, pp. 762–768. May 2003.

[4] R. J. Yang and S. I. Liu, "A 40–550 MHz harmonic-free all digital Delay locked loop using a variable SAR algorithm", IEEE J. Solid-State Circuits, vol.42, no. 2, pp. 361–373. Feb 2007.

[5] R. J. Yang and S. I. Liu, "A 2.5 GHz all digital delay locked loop in 0.13 mm CMOS technology", IEEE J. Solid-State Circuits, vol. 42, no.11, pp. 2338–2347. Nov 2007.

[6] L. Wang, L. Liu, and H. Chen, "An implementation of fast-locking And wide-range 11-bit reversible SAR DLL", IEEE Trans.Circuits Syst. II,Exp. Briefs, vol. 57, no. 6, pp. 421–425. Jun 2010.

[7] David De Caro, "Glitch Free NAND-Based Digitally Controlled Delay Lines", IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 21, no. 1, Jan 2013.

[8] A. G. M. Strollo, D. De Caro, E. Napoli, and N. Petra, "A novel high speed sense amplifier based flip-flop", IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 11, pp. 1266–1274, Nov. 2005.

[9] D. D. Caro, C.A.Romani, N.Petra, A.G.M.Strollo and C.Parrella, " A 1.27 GHz, all digital spread spectrum clock generator/synthesizer in 65 nm CMOS", IEEE J. Solid-State Circuits, vol. 45, no. 5, pp. 1048–1060.May 2010.