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A Self Calibrated Based Clock Generator for DLL

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Abstract — In this paper, a Delay-Locked Loop (DLL) based clock generator is designed which can be used mainly for dynamic frequency scaling. This DLL-based clock generator is found to have low-jitter and can provide the system clock with frequencies in the range of 0.5 to 8 times of reference clock, depending on the workload of the EISC processor. This proposed analog self-calibration method and a phase detector with an auxiliary charge pump can effectively reduce the delay mismatch between the delay cells in the voltage-controlled delay line and the static phase offset due to the current mismatch in the charge pump, respectively. Power and delay mismatches are analyzed by using delay calibration method and by using alpha latch instead of delay calibration. It is found that the performance parameters like power and area are better reduced while using alpha latch rather than delay calibration.

***Index Terms* — Calibration, delay-locked loop (DLL), dynamic frequency scaling (DFS), extendable Instruction set computing (EISC).**

I. INTRODUCTION

The extendable instruction set computing (EISC) processor has been used for several portable multimedia applications. Handheld applications usually use a battery as the power source, which stores a limited amount of energy. The limited amount of energy introduces the problem of power constraints. Hence, portable applications should be designed to consume less power to extend the lifetime of the battery. A dynamic voltage and frequency scaling (DVFS) scheme can support the realization of an energy-efficient embedded processor. Similarly, according to the workload of the EISC processor, a DC-DC buck converter and a delay-locked loop (DLL)-based clock generator can change the supply voltage and the system clock frequency, respectively. By doing so, the EISC processor can be managed to Consume energy efficiently. However, embedded processors for mobile applications tend to be exposed to various harsh environments. Especially, supply voltage fluctuations and timing reservations caused by process, voltage, and temperature (PVT) variations can significantly degrade the performance of the processor. Thus, the susceptibility of the clock generator to external noise and on-chip variations must be addressed to achieve high performance. The proposed clock generator uses a DLL employing an edge-combining type of frequency multiplication scheme. Since the edge-combiner- based clock generator uses multiphase clocks from the voltage- controlled delay line (VCDL) to produce the output clock, the delay between each delay cell in the VCDL should be made equal to achieve an accurate output frequency. However, PVT variations and device mismatch can cause a delay mismatch in the VCDL, which leads to poor jitter performance of the output clock. Current mismatch in the charge pump results in a static phase offset, which also deteriorates the performance of the clock generator. To reduce the influence of such on-chip variability, novel circuit techniques have been required. A methodology to compensate for the delay mismatch, which is inevitable under PVT variations, is presented along with a new analog calibration scheme. A phase detector that incorporates an auxiliary charge pump is also proposed to reduce static phase offset. In addition, a lock detector is proposed to minimize unnecessary power dissipation. An overview of this paper is as follows. Section II describes the overall architecture of the proposed clock generator and Section III presents its circuit implementation. The key benefit of the proposed idea is demonstrated through experimental measurement in Section IV. We estimate our results and calculation for power in section V. Conclusions are presented in Section VII.

II. OVERVIEW ARCHITECTURE

The entire architecture of the proposed DLL-based clock generator is shown in FIGURE I. To take advantage of the fully differential VCDL, a single-to-differential converter (S2D) converts the reference clock into a differential clock. The core DLL produces 16 pairs of multiphase clocks, which are used for frequency multiplication. The multiphase clocks from the VCDL pass through a self-calibration loop consisting of a timing error comparator and a delay calibration buffer.

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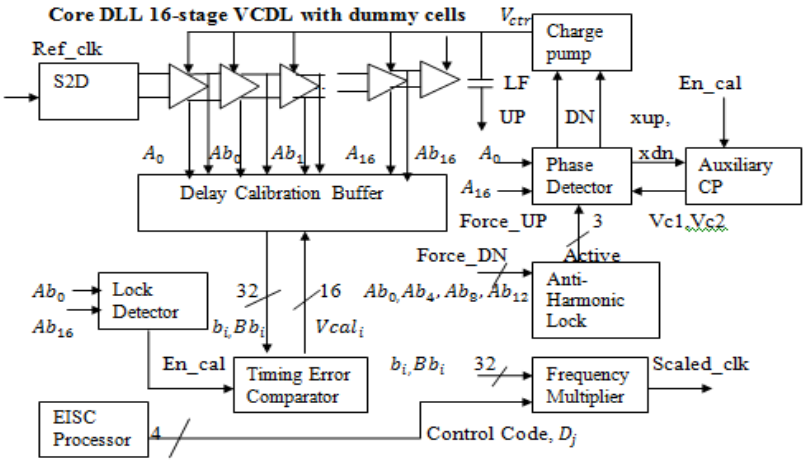

Fig I : Proposed Self-Calibrated DLL-Based Clock Generator

Depending on the thermometer code from the EISC processor, the frequency multiplier selects and merges short pulses that are generated with the calibrated multiphase clocks. The merged short pulses create a scaled system clock of a desired frequency with a 50% duty cycle through a toggled-pulsed latch. Since multiphase clocks are used for frequency multiplication, an anti-harmonic lock circuit is adopted to prevent the core DLL from locking at more than one reference clock cycle. Without an anti-harmonic lock circuit, the frequency multiplication ratio can be incorrect and can bring about the total failure of clock synthesis. A phase detector (PD) with an auxiliary charge pump reduces the static phase offset, which can cause a spur in the output clock. The lock detector can discern the moment that two input clock edges to the PD are brought into very close alignment. To avoid excessive power consumption, the lock detector enables the delay mismatch calibration and the static phase offset compensation after the core DLL acquires lock. The clock generator uses a 15 MHz clock as the reference clock and gives the EISC processor a 30MHz clock as the nominal system clock with frequency multiplication of two.

III. CIRCUIT IMPLEMENTATION

A. DELAY MISMATCH SELF-CALIBRATION

In practice, the temporal positions of the multiphase clocks in the VCDL can digress from their ideal positions due to external noise and on-chip variations. This digression can increase the timing jitter in the multiplied output clock. Therefore, the delay mismatch problem must be solved especially in its relation to multiphase-using clock generators. Several calibration schemes have been proposed in the literature to deal with the delay mismatch issue. However, a finite quantization error of the digital calibration can still limit the calibration resolution. More circuit complexity and chip area should be spent to reduce the quantization error. The analog calibration loop in can affect the loop behavior of the core DLL since the calibration loop adjusts the delay in the main voltage-controlled oscillator (VCO) directly. Also, the calibration loop cannot calibrate all the multiphase clock signals simultaneously. Consequently, the weakness of conventional self-calibration schemes necessitates an enhanced approach. The proposed analog self-calibration loop consists of a delay calibration buffer and a timing error comparator. The delay calibration buffer consists of 16 separate delay calibration buffer cells shown in FIGURE II and receives multiphase clocks from the VCDL. Each delay calibration buffer cell consists of a two-stage delay cell with small delay coverage. The schematic of the proposed timing error comparator is shown in FIGURE II (a). Each timing error comparator cell compares three successive multiphase clocks from the delay calibration buffer. The timing diagram of the delay calibration buffer is shown in FIGURE II (b).

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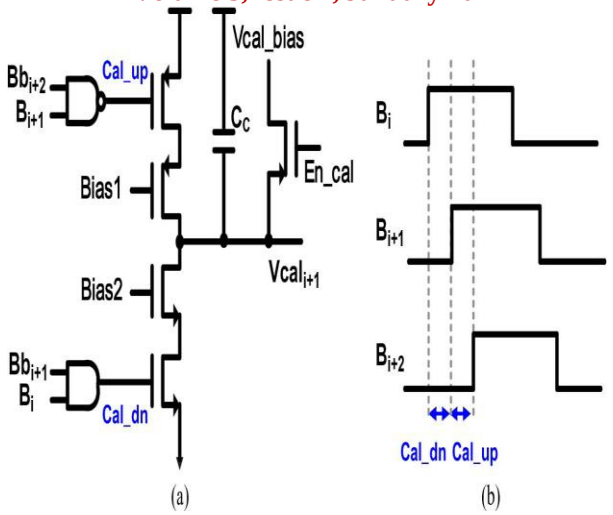

Fig II: (a) Timing Error Comparator Cell (b) Timing Diagram Of Delay Buffer Output

The timing error comparator compares the relative pulse widths of Cal_dn and Cal_up, which are the signals indicating the phase difference between adjacent multiphase clocks. Then, it periodically charges or discharges the capacitor, Cc (2.5 pF) according to the pulse widths of Cal_dn and Cal_up. The control voltage Vcal_{i+1} is fed back to the delay buffer to adjust the delay of in order to place right in the middle of the two adjacent multiphase clocks. The current mismatch of timing error comparator is the limitation of this recompense method. By calibrating not the VCDL outputs directly, but, the delay calibration buffer outputs, the proposed self-calibration scheme can reduce the delay mismatch without affecting the core DLL loop behavior. In addition, since the proposed scheme uses an analog calibration method instead of a digital counterpart, the circuit does not suffer from a finite digital quantization error. Because of these advantages, the delay mismatch can be effectively calibrated to improve the jitter performance. To determine the calibration range of the self-calibration scheme and optimize the area occupied by the self-calibration circuit, a 100-point Monte Carlo simulation for the VCDL was conducted. In the simulation, the input frequency was 15 MHz and the threshold voltage was assumed to have 100 mV variations. FIGURE II shows the delay deviation statistics with about 600 ps of possible maximum delay mismatch. Thus, the delay calibration buffer cell is designed to cover up to at least 600 ps. Through the Monte Carlo simulation, the area penalty of the self-calibration circuit can be minimized and the required delay range for delay mismatch compensation can be guaranteed.

B. STATIC PHASE OFFSET COMPENSATION

Current mismatch in the charge pump is the main cause of the static phase offset between A_0 and A_{16} . Several solutions to alleviate the static phase offset have been investigated. However, it is still hard to completely remove this mismatch solely by manipulating the charging or discharging current of the main charge pump under the PVT variations. Thus, the compensation for the mismatch should be approached differently. The proposed phase detector incorporating an auxiliary charge pump is shown Fig. 3. After the core DLL is locked, the auxiliary charge pump begins its operation. The auxiliary charge pump is a simple charge pump that can generate two control voltages,V_{C1} and V_{C2} , using internal UP and DN pulses, xup and xdn , and their complementary signals, $xupb$ and $xdnb$. The two control voltages, V_{c1} and V_{c2}, generated on the auxiliary capacitors, C_{AUX1} and C_{AUX2} (11 fF respectively) are fed back to the gates of S_1 and S_2 in the phase detector and they adjust the transconductance of S_1 and S_2. For example, if the static phase error Δt, exists between A_0 and A_{16}, V_{c1} decreases and V_{c2} increases, as shown in FIGURE III(a). The increasing gradually turns on and it competes against the driving ability of the Inv_2 when xdn tries to rise, while V_{c1} almost turns off.

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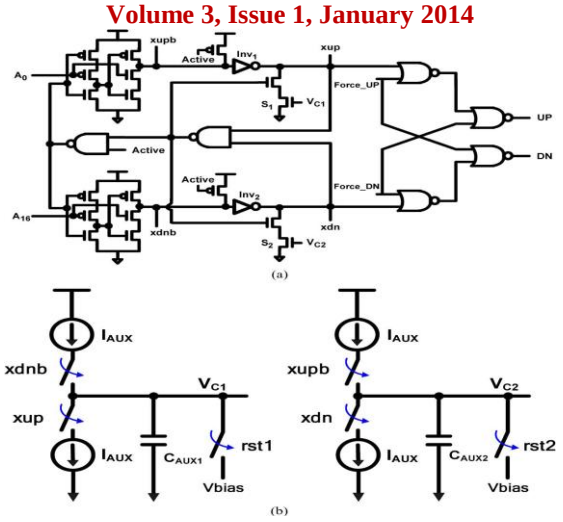

Fig III: (a) Phase Detector and (b) Auxiliary Charge Pump.

As a result, the slew rate is slow, as described in FIGURE III(a), and the difference between the charging and discharging current caused by the pulses increases. Then, the DLL reduces the delay of the feedback clock, A_{16}, diminishing the static phase offset. Meanwhile, the two control voltages, V_{c1} and V_{C2} , are reset to $Vbias$ by $rst1$ and $rst2$ respectively, to prevent them from saturating at VDD or GND as shown in FIGURE III(b). By the proposed compensation technique, the static phase offset between A_0 and A_{16} , due to a current mismatch in the main charge pump can be effectively mitigated without adding complicated circuitry.

C. LOCK DETECTOR

Delay mismatch calibration should begin after the core DLL is locked so that the timing error comparator can detect the exact amount of phase error to be calibrated. If the self-calibration circuit operates before the core DLL is locked, the calibration may go in the wrong direction, which would necessitate a lock detection circuit. Static phase offset compensation also needs to be started after locking to detect and adjust the phase error correctly. As shown in FIGURE IV, the proposed lock detector measures the delay between the two clocks, and from the VCDL. If the measured delay is smaller than the predetermined delay, the lock detector activates both the delay mismatch calibration and the static phase offset compensation, respectively. Since the timing comparators and the auxiliary charge pump operate only after the core DLL is locked, the initial calibration error and additional power dissipation can be avoided.

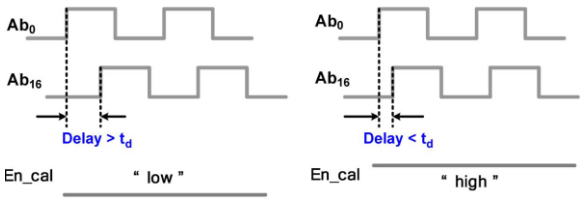

Fig IV: Lock Detector and Its Timing Diagram before and After Locking.

IV. MEASUREMENT RESULTS

The prototype of the self-calibrated DLL-based clock generator was implemented in a 0.18- m CMOS process. The chip micro photo of the dynamic frequency scaling (DFS) circuit along with the EISC processor and the DVS circuit. The fabricated DLL-based clock generator occupies 0.27 mm of active area and consumes 15.56 mA at 120 MHz The multiplied output waveforms with a 15 MHz reference clock. The measurement results verified that the output clock frequency of the clock generator was dynamically scaled by the digital thermometer code with the aid of the proposed self-calibration scheme, the RMS jitter of the output clock was reduced from 11.1 to 9.7 ps. The normalized power consumption of the EISC processor in several DVFS modes. The result demonstrated that the proposed DFS circuit can effectively save battery energy and extend battery lifetime by reducing the dynamic power dissipation of the EISC processor. The performance characteristics of the proposed DLL-based clock generator and compares them with thus of conventional DLL-based clock

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generators. The proposed self-calibrated DLL-based clock generator occupies the smallest active area among those with a self-calibration circuit and exhibits excellent jitter performance.

V. RESULT AND CALCULATION

RESULT OF SELF CALIBRATED DLL

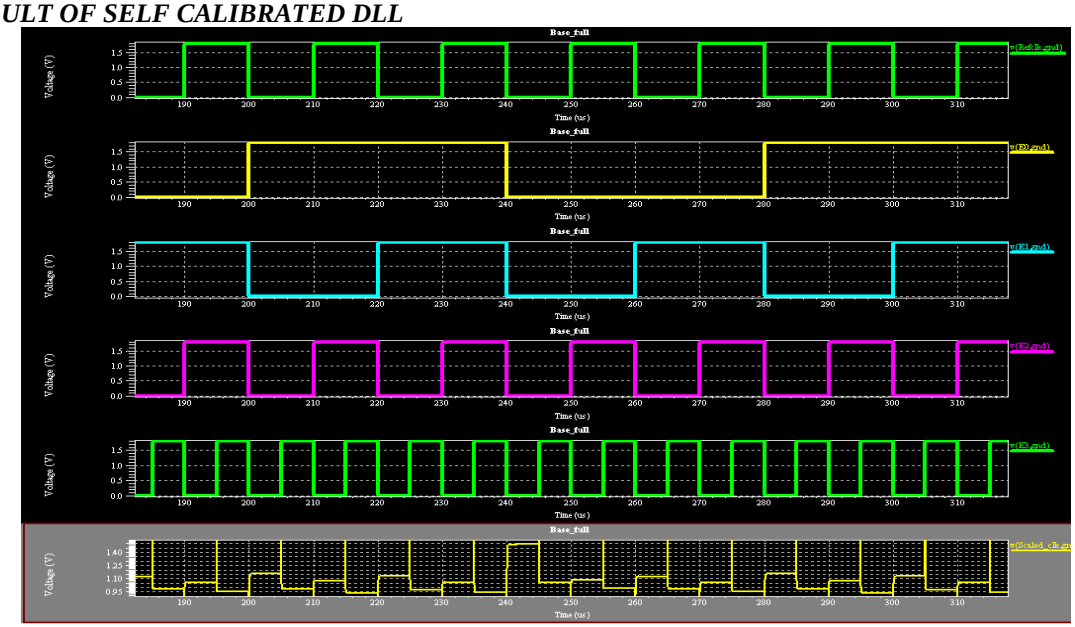
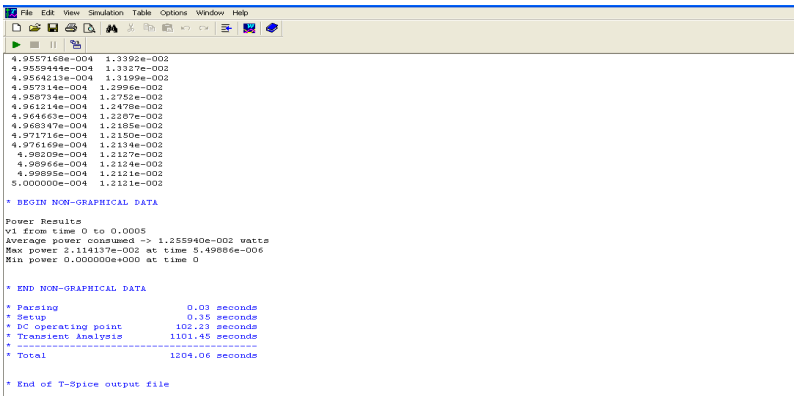


Fig VI: Result of Self Calibrated DLL

FIGURE VI: Shows result of self calibrated DLL which describes about power and delay Mismatching.

CALCULATION FOR POWER



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File  Edit  View  Simulation  Table  Options  Window  Help

 4.9557168e-004  1.3392e-002
 4.9559444e-004  1.3327e-002
 4.9564213e-004  1.3199e-002
 4.957314e-004  1.2996e-002
 4.958734e-004  1.2752e-002
 4.961214e-004  1.2478e-002
 4.964663e-004  1.2287e-002
 4.968347e-004  1.2185e-002
 4.971716e-004  1.2150e-002
 4.976169e-004  1.2134e-002
  4.98209e-004  1.2127e-002
 4.989966e-004  1.2124e-002
  4.99895e-004  1.2121e-002
 5.000000e-004  1.2121e-002

* BEGIN NON-GRAPHICAL DATA

Power Results
v1 from time 0 to 0.0005
Average power consumed -> 1.255940e-002 watts
Max power 2.114137e-002 at time 5.49886e-006
Min power 0.000000e+000 at time 0


* END NON-GRAPHICAL DATA

* Parsing                    0.03 seconds
* Setup                      0.35 seconds
* DC operating point        102.23 seconds
* Transient Analysis       1101.45 seconds
* ------------------------------------------
* Total                     1204.06 seconds


* End of T-Spice output file
```

Fig VII: Calculation for Power

VI. CONCLUSION

A low-jitter DLL-based clock generator employing an advanced self-calibration technique was presented in this paper. This proposed clock generator can produce an output clock that varies its frequency. This analog calibration with a delay calibration buffer and a timing error comparator can mitigate the delay mismatch and achieves low jitter in spite of on-chip variations. The phase detector in conjunction with an auxiliary charge pump can effectively reduce the static phase offset, boosting the precision of the frequency multiplication. The lock detector can prevent unnecessary power consumption and initial calibration error by enabling the calibration circuits after locking of core DLL. The self-calibrated DLL-based clock generator is implemented with alpha latch instead of delay calibration in order to reduce the power consumption and area considerably. It can support an energy- efficient embedded processor by providing a clean system clock even under harsh

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environment. Therefore, the proposed clock generator can be an attractive choice for dynamic power management of mobile applications. In addition, the Modified VCDL output generator generates the output clock of this DLL and the DLL is under phase tracking. The VCDL output generator is composed of two D flip flops, an AND gate and a clock buffer. The rising edge of becomes the rising edge of and the rising edge of becomes the falling edge of. To increase the control voltage, the rising edge of will be delayed and the delay of the VCDL is increased. Thus, the output clock of the DLL is also delayed. In the steady state, the rising edges between reference clock and output of the DLL are in-phase and the corresponding phase difference is eliminated. Note that the delay range of the VCDL is proportional to the low-level pulse width of. So, it is proportional to the control voltage and the ratio of in the pulse to saw tooth converter, respectively. It means a wide range delay is achieved if the low-level pulse width of is large. Theoretically, the delay range can be close to one period of the input clock.

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