ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 2, Issue 5, September 2013

Hardware Implementation of EZW based Image Compression with Huffman coding

Aiswarya S, Dr. S. Veni
Student (M.Tech VLSI Design), Associate Professor, Amrita Vishwa Vidyapeetham
Coimbatore - 641112

Abstract- ***Embedded Zero-tree Wavelet (EZW) is a wavelet based image compression scheme. It is basically a quantization stage that incorporates some characteristics of the wavelet decomposition. The EZW approach and its descendants significantly outperform some of the generic approaches. The wavelet coefficients in different sub bands represent the same spatial location in the image. This is an important characteristic used by EZW. In case of decomposition, since the size of the different sub bands is different, then a single coefficient in the smaller sub band may represent the same spatial location as multiple coefficients in the other sub bands. This paper describes hardware implementation of EZW encoding algorithm along with Huffman encoding and decoding architectures. After performing lifting based DWT technique and EZW algorithm, Huffman coding ensures further compression of the image. In Huffman coding no bit string is a prefix of any other bit string. Hence each code is uniquely decodable.***

Index Terms- **Embedded Zero-tree Wavelet (EZW), Huffman encoder and decoder, VLSI Architecture.**

I. INTRODUCTION

Digital images require huge amounts of space for storage and large bandwidths for transmission [1]. The objective of image compression is to reduce irrelevance and redundancy of the image data in order to be able to store or transmit data in an efficient form [2]. Wavelet based algorithms Embedded Zero-tree Wavelet (EZW), Set Partitioning In Hierarchical Trees (SPIHT) and Embedded Block Coding with Optimized Truncation (EBCOT) have dominated in image compression [3]-[4]. EZW is computationally very fast among the best image compression algorithm known today. The motivation behind this work has come with reference to Dr. K. P. Soman [5] in which it is mentioned that EZW output can be further compressed using Huffman coding.

Wavelet transforms are the most powerful and most widely used tool to arise in the field of signal processing. Apart from image and video compression EZW finds applications in water marking, face and iris recognition, remote sensing and medical applications like EEG, ECG [6]-[9]. Vijaya Prakash. A.M and K.S. Gurumurthy [10] proposed Low Power VLSI architecture for image compression, which uses Variable Length Coding method to compress JPEG signals. Gopal Lakhani [11] proposed modified JPEG Huffman coding in which they obtained average code reduction to the total image size by their method as 4%.Their methods can be used for progressive image transmission. EZW with Huffman coding was attempted yet. Hence, a technique for image compression using EZW based image compression with Huffman coder is proposed in this work [10]-[11]. Lifting based scheme is well suited for Discrete wavelet transform (DWT) since it requires far fewer computations [12]-[13].

DWT coefficients of the image which is to be compressed were computed using MATLAB software as an initial step. DWT matrix obtained for an n x n image will be having a size of n x n. Fig.1 shows DWT coefficients of 8 x 8 image. After computing DWT matrix, coefficients are scanned in particular order in order to apply image compression algorithm. Image scan methods, based on Raster order or Morton (Z) order are widely used. Morton order is used here since pattern of scanning is same in all frequency bands [14].

57	-35	52	8	5	12	-10	5
-29	25	14	-14	3	1	5	-2
15	15	2	-9	8	-10	6	12
-10	-6	-11	7	7	-2	4	5
-2	12	-1	47	6	6	-2	3

ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 2, Issue 5, September 2013

0	3	-2	1	1	-4	3	1
0	-4	8	-4	4	5	3	3
5	14	4	3	-2	5	-4	1

Fig.1 DWT Coefficients

Generalized form of Morton scan can be obtained by using the expressions as shown in the Fig.2. Where x represents the Morton order of low frequency band of coefficients and n is the order, which represents the size of the image. For an 8 x 8 image, x represents the Morton order of low frequency components which is a 4 x 4 matrix as shown in Fig.3.

x	x+(n/2)(n/2)
x+2(n/2)(n/2)	x+3(n/2)(n/2)

Fig.2 Morton Scan generic format

1	2	5	6
3	4	7	8
9	10	13	14
11	12	15	16

Fig.3 The Morton order of lowest frequency coefficients (x) for 8 x 8 image

The relationship between each coefficient in each band can be generalized as follows:

LLn – Approximation which is same as the lowest frequency coefficients order or x

HLn – Horizontal Detail or x + (n/2) (n/2)

Here we need to add (n/2) (n/2) with x in order to obtain morton scan order. Since n here is 8, we have to add x with (8/2)(8/2) = 16.

LHn – Vertical Detail or x +2 (n/2)(n/2)

Here we need to add 2(n/2)(n/2) with x in order to obtain morton scan order. Since n here is 8, we have to add x with 2(8/2)(8/2) = 32.

HHn – Diagonal Detail or x +3 (n/2)(n/2)

Here we need to add 3(n/2)(n/2) with x in order to obtain morton scan order. Since n here is 8, we have to add x with 3(8/2)(8/2) = 48.

The resulting Morton scanning order for an 8 x 8 image is shown in Fig.4.

1	2	5	6	17	18	21	22
3	4	7	4	19	20	23	24
9	10	13	14	25	26	29	30
11	12	15	16	17	28	31	32
33	34	37	38	49	50	53	54

ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 2, Issue 5, September 2013

35	36	39	40	51	52	55	56
41	42	45	46	57	58	61	62
43	44	47	48	59	60	63	64

Fig.4 Morton Scan order for 8 x 8 image

Based on EZW algorithm, by scanning through the DWT coefficients in Morton order, combination of four symbols is assigned that are P, N, Z and T as per [15].

II. EZW ALGORITHM

Threshold is initialized by $T_0 = 2^{\lfloor \log 2(C_{max}) \rfloor}$ (1)

where C_{max} is the maximum of the absolute value of the DWT coefficients. In EZW algorithm entire wavelet coefficient matrix is scanned in order to find out the maximum value of the coefficient. C_{max} for the image shown in Fig.1 is computed as 57. We can infer from the computed coefficients for any image that maximum value of coefficient occurs at the lowest frequency sub band (LL band). So we need not check the entire coefficient matrix in order to find out the maximum value of the coefficient which can reduce the computational complexity.

Threshold T is an indicator that specifies bit position. T is the current quantization width. In each iteration width is divided by 2, so another less significant bit of the coefficients becomes known. In EZW algorithm each iteration consists of a dominant pass (principal stage) followed by a subordinate pass (secondary stage). In dominant pass coefficients from the dominant list (i.e. Entire wavelet coefficients) are tested for significance with the current threshold. A digital magnitude comparator can be used to compare and generate the results.If a coefficient is found significant, then

1) It's sign is determined
2) It is classified as either P [00] or N [01]
3) It's magnitude is appended to subordinate list.

Otherwise, assign symbol Z [10] or T [11] to insignificant wavelet coefficient. Based on this, the Wavelet coefficients are coded as follows:

(i) ***P*** if the coefficient is positive and has an absolute value greater than threshold.
(ii) ***N*** if the coefficient is negative and has an absolute value greater than threshold.
(iii) ***Z*** if the coefficient is less than threshold but if one of its children has an absolute value greater than threshold.
(iv) ***T*** if the coefficient is less than threshold and if all its children have absolute values less than threshold. These symbols are obtained after performing dominant pass of EZW.

Table . 1 shows the symbols obtained after performing EZW (Embedded Zerotree wavelet) coding algorithm for the wavelet coefficients shown in Fig.1 during dominant pass.

Table.1 Symbols of the wavelet coefficients for the dominant pass

Threshold	Dominant pass result
32	P N Z T P T T T T Z T T T T T T T P T T
16	Z T N P T T T T T T T T
8	Z Z Z Z Z P P N P P N T T N N P T P T T N T T T T T T T T P T T T P T T T T T T T T T T P T T T T T T T T T T T T T T T T

ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 2, Issue 5, September 2013

4	Z Z Z Z Z Z Z T Z T Z N Z Z Z Z P T T P T P P T P N P T N T T T T T P T P N P P P P T T T T T P T P T T T T P N P
2	Z Z Z Z Z T Z Z Z Z Z T P Z Z Z T T P T T T T N P T P P T T P T T T T N P P N T T T T P N N P T T P T T P P T T T

Table.II shows the bits obtained after performing EZW (Embedded Zerotree wavelet) algorithm for the wavelet coefficients shown in Fig. 1 during subordinate pass.

Table.II Bits of the wavelet coefficients for the subordinate pass

Threshold	Subordinate pass result
32	1010
16	100111
8	0011100111100010001110
4	0101000111110101010010110001100000001100000
2	1101110001101100000000011111001010000001100100010101101 1

In hardware point of view since there are four symbols, each symbol can take two bits for representation. So P is coded as 00, N as 01, Z as 10 and T as 11. Then these symbols are encoded using a statistical encoding technique called Huffman coding for further compression. The decoding phase of EZW consists of reversing the above stages.

(1) Initialization: Initialize the values of the coefficients by zeros, the list of coefficients processed by an empty list and the threshold by *Tn.*

(2) Principal stage: Read the codes of the principal list one by one. Each code is one of the four symbols [*P*, *N*, *Z*, *T*]:
- If the code is *P*, assign *Tn* as the value of the coefficient and add the coefficient (its position) to the list of Processed coefficients;
- If the code is *N*, assign - *Tn* as the value of the coefficient and add the coefficient to the list of processed Coefficients;
- If the code is *Z* or *T*, do nothing.

(3) Secondary stage: Read the codes of the secondary list one by one. It corresponds to the list of already processed coefficients.

For each of these coefficients, if the corresponding term of the secondary list is zero, do nothing, whereas if this term is 1 modify its value. If the coefficient is positive, then ½(*Tn*-1) is added to it. If it is negative the same quantity can be subtracted from it.

(4) Updated new threshold : We can calculate the new threshold with $Tn+1= (1/ 2)Tn$

The algorithm steps for the proposed scheme are given in the flow chart shown in Figure. 5. The proposed architecture modules are explained in section III.

ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 2, Issue 5, September 2013

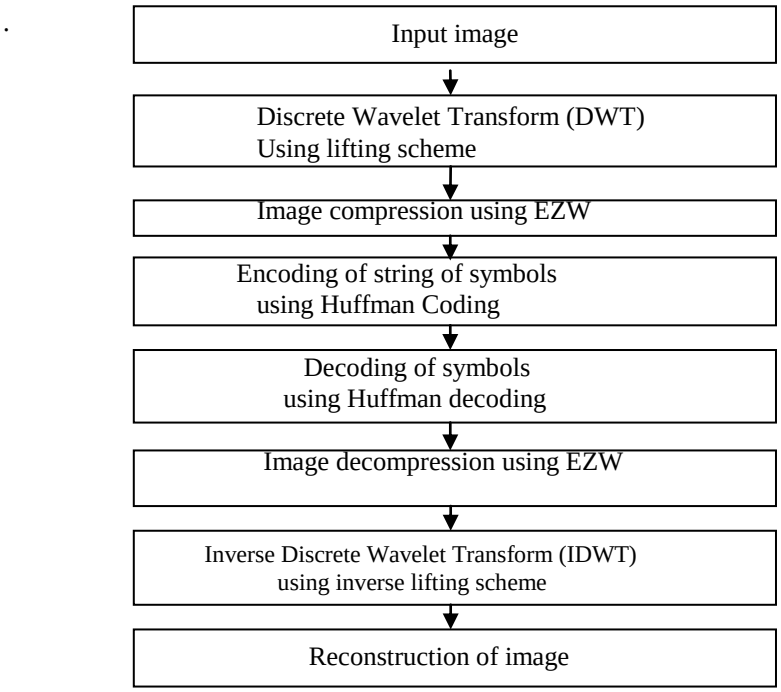

Fig. 5 Flow Chart

III. HUFFMAN CODER ARCHITECTURE

Huffman encoding is an algorithm or lossless data compression that represents data in fewer bits than otherwise needed. Huffman coding needs to prepare a code word table that contains the information of mapping data between real data and the code words for encoding. There are two types of Huffman coding methods: static Huffman is coding and adaptive Huffman coding. Static Huffman coding uses a known code word table for encoding. While, Adaptive Huffman coding uses an encoding tree which is adaptively constructed and maintained at sender as well as receiver side. Here we use static Huffman coding in our algorithm to encode the symbols P, N, Z and T. After performing lifting based DWT and EZW for different images we came to a conclusion that symbol T occurs more frequently among the four symbols. Hence, one bit is assigned to the symbol T i.e 0 or 1. Based on the order of occurrence of the symbols Z, N and P, the binary bits are assigned as follows.

P is encoded as 1110
N is encoded as 110
Z is encoded as 10
T is encoded as 0.
We can also use the following bits.
P is encoded as 0001
N is encoded as 001
Z is encoded as 01
T is encoded as 1.

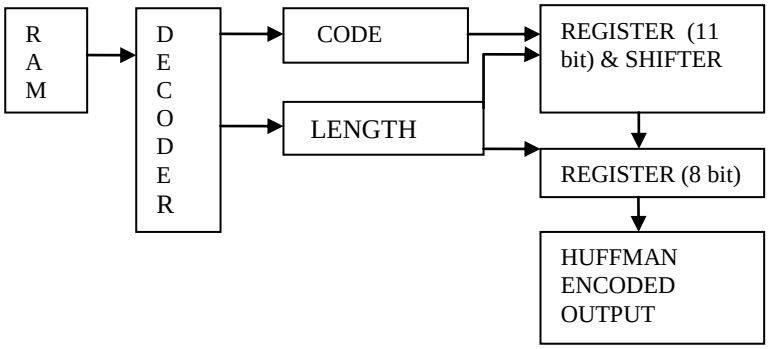

Fig. 6. Huffman encoder architecture

ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 2, Issue 5, September 2013

The working modules of the proposed architecture are shown in Fig.6. Bit strings corresponding to symbols P, N, Z and T are stored in a RAM. The decoder reads these bit strings and generates a code and a length for each symbol, where code represents the Huffman encoded codes like 1110, 110, 10 and 0 or 0001, 001, 01, and 1, corresponding to P, N, Z and T symbols respectively. Length represents number of bits in the Huffman code. For example length for symbol P is 4 and for symbol N is 3. The coded bit strings are stored in a 11 bit register and each time when register is filled with eight bit positions Huffman encoded string gives an output. An eight bit register is selected because it will represent code for at least two symbols if they both are P symbols. FSM (Finite State Machine) is a mathematical model of computation to design sequential logic circuits. Event driven FSM represents transition from one state to another and is triggered by an event (Huffman code). Huffman decoder is modeled as a Finite State machine having 7 states S0, S1, S2, S3, S4, S5, S6 as shown in Figure.7. It is basically an infinite loop that reads incoming events. The state machine has only two states: ***State*** and ***Next state***. It represents a mealy machine that is outputs are dependent of inputs and states.

States S0, S2, S4, S6 outputs corresponding code. State S0 detects symbol P, State S2 detects symbol N, State S4 detects symbol Z and State S6 detects symbol T and outputs 00, 01, 10 and 11 respectively. Ones and zeros represents the inputs to each of the 7 states.

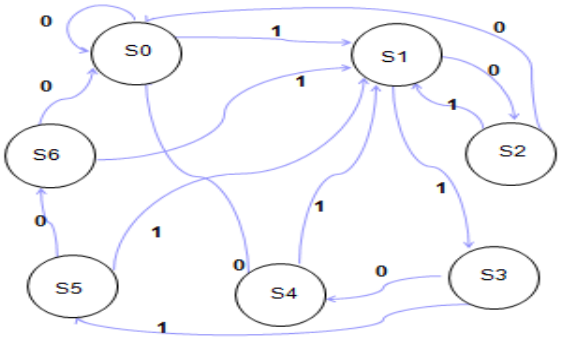

Fig.7 Huffman decoder

IV. RESULTS AND DISCUSSIONS

EZW encoder and Huffman coder are implemented and simulated on iverilog. MATLAB simulation result of subordinate pass for threshold 16 and 32 for Fig.1 is shown in Fig.8 and Fig.9 respectively.

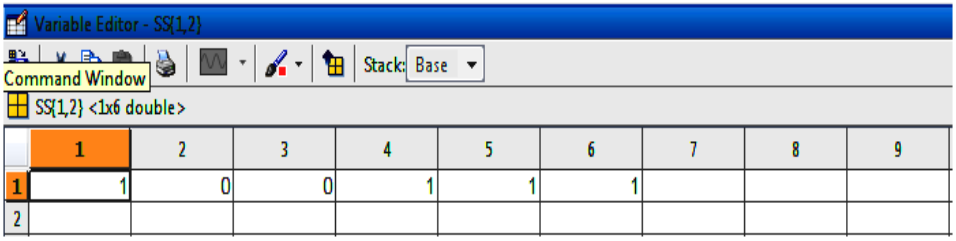

Fig.8. MATLAB Simulation result of subordinate pass for threshold 16

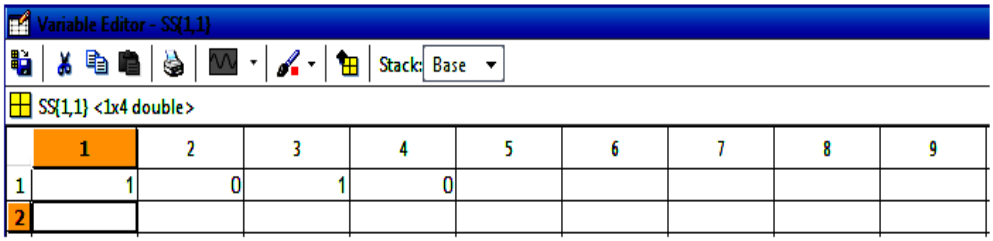

Fig.9. MATLAB Simulation result of subordinate pass for threshold 32

ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 2, Issue 5, September 2013

Fig. 10, 11 and 12 shows the simulation waveform of EZW encoder for threshold 16, Huffman encoder and decoder respectively.

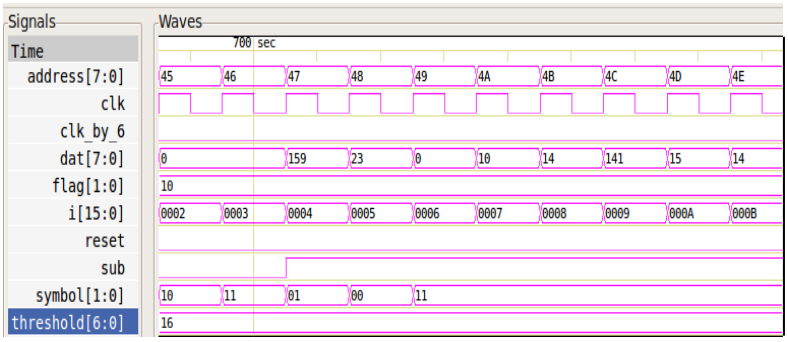

Fig.10. Simulation waveform of EZW encoder for threshold 16 on iverilog

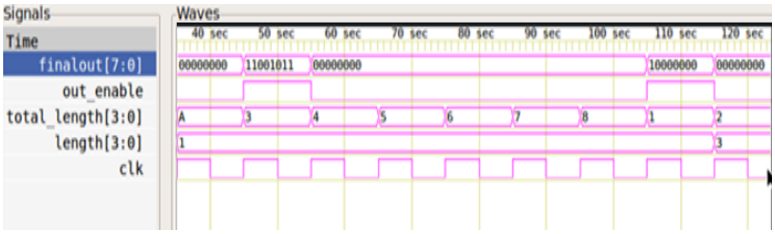

Fig.11. Simulation waveform of Huffman encoder for threshold 16 on iverilog

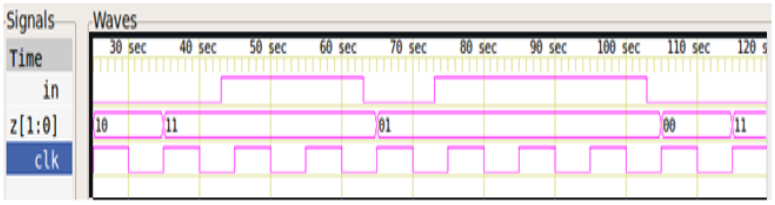

Fig.12. Simulation waveform of Huffman decoder for threshold 16 on iverilog

The power analysis results of EZW encoder are listed in the following Table. III

Table.III Power analyzer summary

Power play power analyzer status	Successful
Quartus version	11.0 Build157 04/27/2011 SJ Web edition
Top level entity name	EZW
Family	Cyclone II
Device	EP2C5T144C6
Power models	Final
Total thermal power dissipation	34.81mW
Core static thermal power dissipation	18.02 mW
I/O thermal power dissipation	16.79 mW

ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 2, Issue 5, September 2013

The quality of the designed VLSI architecture for Huffman encoder and decoder, are measured using PSNR value and bits per pixel. The results are listed in the following Table. IV and Table.V for 8 x 8 image and 16 x 16 image respectively.

Table IV Compression ratio and PSNR values (8 x8 image)

Threshold	No of bits needed	Bits per pixel (bpp)	PSNR (dB)	Compression ratio
32	33	0.25	25.8925	15.06
16	51	1.12	26.6137	9.85
8	91	2.75	27.6726	3.41

Table.V Compression ratio and PSNR values (16 x 16 image)

Threshold	No of bits needed	Bits per pixel (bpp)	PSNR (dB)	Compression ratio
32	132	0.37	26.7929	12.11
16	204	1.23	26.9137	10.83
8	364	2.64	27.6526	2.49

V. CONCLUSION

A new architecture for image compression by EZW algorithm with Huffman coder is proposed in this work. The efficiency of the structure is improved in the design by utilizing Huffman coder architecture which is explained in the section II. The reduced hardware complexity of threshold calculation structure is incorporated and is implemented. For DWT coefficient calculation, lifting based scheme is utilized. The proposed structure is scalable for higher number of levels. The single RAM utilization for storage of DWT coefficients helps in reducing the hardware elements by utilizing the same memory for entire calculations. Since this architecture along with Huffman coder increases the compression ratio, without increasing the memory bandwidth, the implementation is suitable for high speed image processing. The architecture can be improved for processing of large size images and further to process video signals.

REFERENCES

[1] Shapiro J.M. “Embedded image coding using zero trees of wavelet coefficients”. IEEE Trans. Signal Proc., Vol. 41, No. 12, pp. 3445-3462, Dec. 1993.

[2] S.P. Raja, Dr. A. Suruliandi, “Analysis of Efficient wavelet based Image Compression Techniques,” Second International conference on Computing, Communication and Networking Technologies”, 2010.

[3] Kai Liu, Evgeniy Belyaev, and Jie Guo “VLSI Architecture of Arithmetic Coder Used in SPIHT” IEEE Trans. on VLSI Systems, Vol. 20, No. 4, pp. 697-710, Apr. 2012.

[4] Ganesh Bhokare, Ujjwal Kumar, Bhushan Patil and Vikram Gadre “Efficient coding of sparse trees using an enhanced - embedded zero tree wavelet algorithm” SIViP pp.99–108, Jul.2012.

[5] Dr. K. P. Soman and Dr. Ramachandran K.I., “Insight into wavelets -From Theory to Practice”, Prentice - Hall India.

[6] Mohammad S. Nambakhsh, Alireza Ahmadian, Mohammad Ghavami, Reza S.Dilmaghani and S. Karim i-Fard “ A Novel Blind Watermarking of ECG Signals on Medical Images Using EZW Algorithm for Image Compression” Proceedings of the 28th IEEE EMBS Annual International Conference New York City, pp.3274-3277, Sept. 2006.

[7] Amany Farag, Randa Atta, and Hani Mahdi “Feature Extraction Based on the Embedded Zero-Tree DCT for Face Recognition” Proceedings of 2010 IEEE 17th International Conference on Image Processing, pp.3813-3817, Sept.2010.

[8] Jian-wei Han, Jian-dong Fang “Research on Remote Sensing Image Compression Based on Lifting Wavelet Transform” International Conference on Multimedia and Information Technology, pp. 205-208, 2008.

[9] Lili Hsieh, Wen-Shiung Chen, Tzung-Hao Li “Personal Authentication using Human Iris Recognition based on Embedded Zero tree Wavelet Coding” 2010 Fifth International Multi-conference on Computing in the Global Information Technology, pp.99-103.

ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 2, Issue 5, September 2013

[10] Vijaya Prakash. A.M1 & K.S. Gurumurthy "Vlsi Architecture For Low Power Variable Length Encoding And Decoding For Image Processing Applications" International Journal of Advances in Engineering & Technology , Vol. 2, Issue 1, pp.105-120, Jan 2012.

[11] Gopal Lakhani "Modified JPEG Huffman Coding" IEEE Transactions on Image Processing, Vol. 12, No. 2, pp.159-169, Feb. 2003.

[12] Kishore Andra, Chaitali Chakrabarti and Tinku AcharyaJ. L. Alqueres and J. C. Praca, "A VLSI Architecture for Lifting-Based Forward and Inverse Wavelet Transform" IEEE Transactions On Signal Processing, Vol. 50, No. 4, pp.966-977, Apr. 2002.

[13] Maria E. Angelopoulou And Peter Y. K. Cheung "Implementation and Comparison of the 5/3 Lifting 2D Discrete Wavelet Transform Computation Schedules on FPGAs" Journal of VLSI Signal Processing, 2007.

[14] Janaki. R, Dr.Tamilarasi.A "Still Image Compression by Combining EZW Encoding with Huffman Encoder" International Journal of Computer Applications (0975 – 8887), Vol. 13 No.7, pp.1-7, Jan 2011.

[15] Vinay U. Kale , Shirish M. Deshmukh "Visually Improved Image Compression by Combining EZW Encoding with Texture Modeling using Huffman Encoder" IJCSI International Journal of Computer Science Issues, Vol. 7, Issue 3, No 11, pp. 28-38, May 2010.

AUTHOR BIOGRAPHY

Aiswarya S has obtained her B. Tech degree from Calicut University during 2011 and M.Tech degree in VLSI Design during 2013 from Amrita Vishwa Vidya Peetham. Her areas of interests are VLSI Design, Signal Processing and Image Processing.

Dr.S.Veni obtained her AMIE degree from Institution of Engineers, Calcutta in 1994 and M.E degree from Coimbatore Institute of Technology, Coimbatore in 1998. She obtained her Ph.D degree in the area of Image Processing from Amrita Vishwa Vidya Peetham in January 2012. Her areas of interest are Signal and Image Processing, VLSI Design. She has 20 years of experience (PG & UG) in teaching field. She has published 20 papers in International Journals and national/International conferences. She has guided more than 20 projects for PG and UG students. She has received best paper award 3 times. She is a member in ISTE, IETE and Associate member in Institution of Engineers.