ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 2, Issue 1, January 2013

Comparative Study of Various Network Processors Processing Elements Topologies

Shuchi Bhagwani
Mtech (CSE), SRCEM Banmore, RGPV

Abstract*— An enormous requirement for high-speed in computer networks due to augmented number of users, servers, connections and high demands for new applications, along with the significant growth in data traffic has claimed the development and deployment of high-speed telecommunication systems. We use specialized processors, called network processors (NPs) to solve these problems. NPs are application specific instruction processors (ASIPs) and are specially designed to perform packet processing tasks. Its architecture is usually a question of different trade-offs between performance, flexibility and price. So it is therefore important to study about NPs processing elements topologies, as well as examine which topology is efficient in terms of performance (Throughput and Utilization ratio). In this paper, we form three types of NPs processing elements topologies, parallel, pipelined and hybrid topology. By analyzing these three topologies our analysis indicate that, while taking into account the throughput and utilization ratio, hybrid and pipeline topologies are best suited over parallel topology.

***Index Terms*— Network Processor, Parallel Topology, Pipeline Topology, Hybrid Topology.**

I. INTRODUCTION

Network processors are intended to provide the performance of traditional ASICs and programmability of general-purpose processors. NP's are system on chips specifically designed to process network packets at very high speed and usually implemented as ASIP.NP's provide important capabilities: Scalability, product differentiation, low cost and faster time to market. Network processor provides a programming interface for implementing packet forwarding services such as routers, switches and firewalls. All NP's are usually composed of: many processing engines (PE's), dedicated hardware accelerators, memory resources, network interfaces and software support. According to Flynn's classification, NP's are MIMD. Commercial NP's are EZChip'sNP-1-4, Intel's IXP1200, 2400, 2800, 2850 NPs, IBM's Power NP, Motorola's C-5 NP.

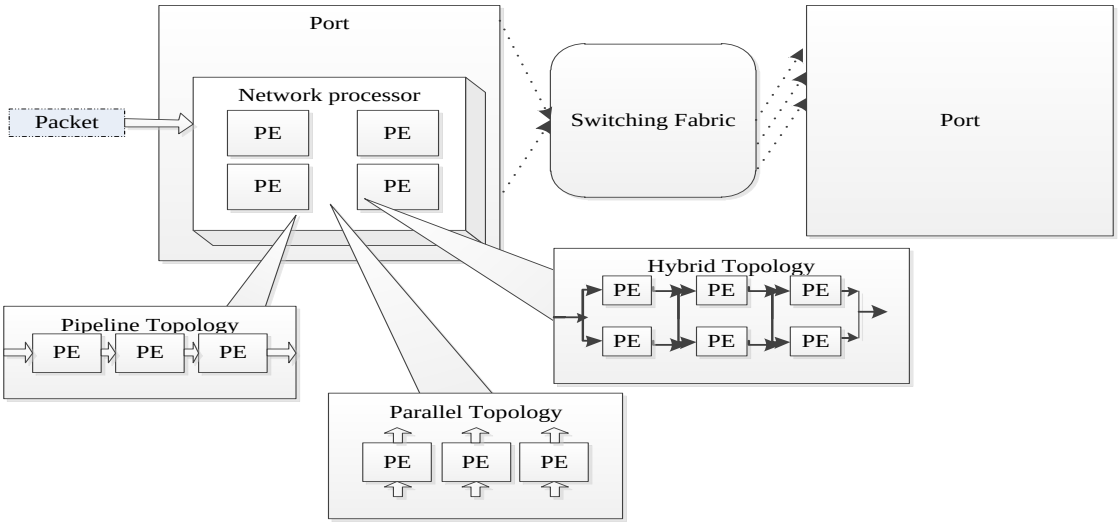

Fig 1: Router System with Network processors .PE's in network processor having three different topologies: Parallel, Pipeline or Hybrid. [6]

ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 2, Issue 1, January 2013

II. RELATED WORK

There are three realms of related work, addressing the modeling of network processors, addressing the programming of network processors, and addressing the evaluation of network processor applications [3]. Now days, we are using a wide variety of network processor designs. Flexibility, programmability, performance, cost, development time and power consumption are trade-offs of these designs [6][7]. NPs provide high processing speed, Adaptability, High level of programmability in network devices. The basic application of network processors is packet forwarding. But beside packet forwarding which previous generations of network routers were focused on, "packet processing" has gained much more importance becoming today's major task. Packet processing is a very general term that could mean a wide range of applications.

III. PROPOSED MODEL

In order to explore different NP topologies and quantitatively obtain the performance of a particular topology, we need to consider the impact of the network processor workload (consisting of a set of "applications") that will be consider in two different packet forwarding applications IPv4 and NAT . For this we use several run time traces. These run time traces are mapped to performance model of network processor for representing workload of packet forwarding application (IPv4, NAT). Performance model is iteratively mapping this workload with different topologies parameters (width, depth etc.) to the generic network processor architecture. By fixing topologies parameters to generic network processor architecture, parallel, pipeline, hybrid topologies can be formed that is mapped to performance model of network processor then finally performance results (throughput, utilization etc.) are gained.

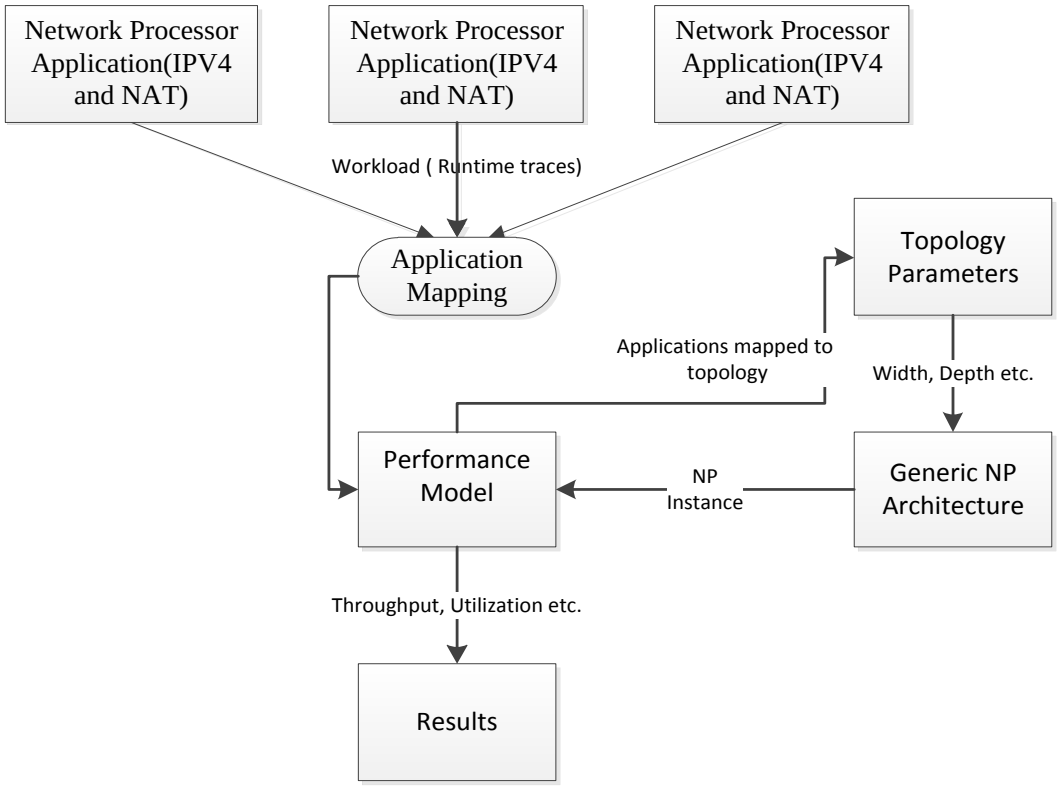

Fig 2: Proposed model

IV. DESIGN EXPLORATION

We have analyzed various network processors, based on this analysis we have come to understand the network processor consist two different types of computational units: processing element (PE's) and micro engine. Computational units are individual processing unit of network processor.

ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 2, Issue 1, January 2013

1. Processing Elements (PE's): Processing element is basis processing unit of network processors. It is an instruction set processor that decodes its own instruction stream.
2. Micro Engine: These are special purpose hardware that is dedicated to perform one specific task also called engine. Micro engines are generally triggered by processing elements.

The basic functional units of the network processor are processing blocks that can be seen as abstractions of PE's. The programming is event-driven in each processing block. When an event occurs, the local processing unit is triggered to run a particular program code in code memory. For example, a packet arrival may trigger the local processing unit to receive the packet from an input port. The packet is processed within the block, and is finally sent to an output port. The packet processing inside a network processor can be divided into two phases: ingress and egress processing phase. Packet enters from ingress phase and then packet is processed by processing blocks and then exit from the egress phase. Some special packets are handled by the route processor, which is called slow path processing. Here we will primarily consider the fast-path processing where packets enter the ingress and are sent directly to the egress. Here we emphasis only on the ingress processing because egress phase requires very less processing capacity as compared to ingress phase.

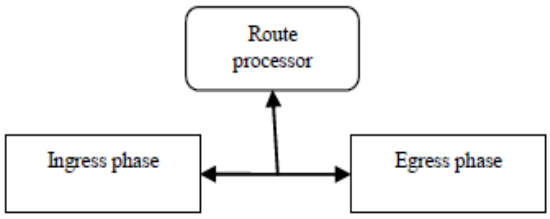

Fig 3: Phases of Network Processor

V. ANALYSING NPs PROCESSING ELEMENT TOPOLOGIES

The analysis of NPs processing element topology requires an abstract representation of NP architecture. We introduce a general NP architecture that allows us to analyze the NP performance and compare their different processing element topologies.

We use a general, parameterized network processor topology shown in Figure 4. The system topology is characterized by three components: processing elements, shared interconnects, and memory interfaces. The packets move from top to bottom. The key parameters are:

The width of the pipeline stage (W), depth of the pipeline stage (D), number of stages per communication interconnect (I), number of memory channels shared by one row of processing elements (M). The variations in these parameters allow our generic NP architecture to represent a wide range of possible NP topologies.

A. Parallel Multiprocessor Based Topology: A parallel topology can be formed by setting the depth (D=1) and I=1, while varying the pipeline width (W) shown in Fig 4.

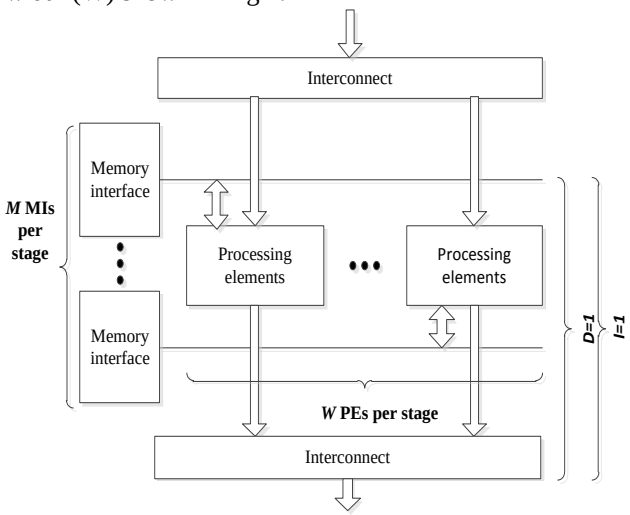

Fig 4: Parallel Multiprocessor Based Topology

ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 2, Issue 1, January 2013

B. Pipeline Multiprocessor Based Topology: A pipeline topology can be formed by setting the width (W=1) and I=1, while varying the pipeline depth (D) shown in Figure 5.

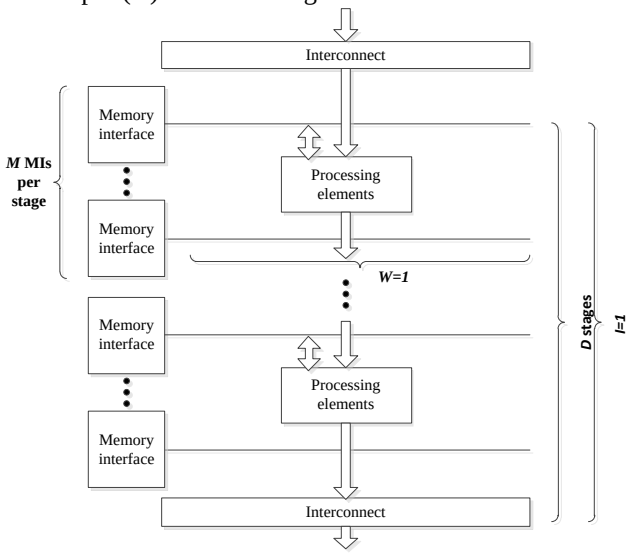

Fig 5: Pipeline Multiprocessor Based Topology

C. Hybrid Multiprocessor Based Topology: Hybrid topology can be achieved by setting pipeline width (W), pipeline depth (D), I=1...D, and M=1...W, to any combination of values. EZchip's NP-1 uses such a topology (W=4, D=4, I=1).Hybrid topology is formed same as parallel and pipeline by varying parameters in generic NP architecture.

VI. CONCLUSION

In this work, we are analyzing the three different NP topologies parallel, pipeline and hybrid topologies by varying different parameters in generic NP architecture and our analysis indicates that pipeline topology outperforms the parallel topology because of less number of packet drops throughput is also high as compared to parallel topology. Initially throughput is low in pipeline topology as compared to the parallel topology but ultimately pipeline topology has higher throughput as compared to parallel topology. Hybrid topology has higher throughput in each processing elements topology but this throughput is increased at certain limit and after this limit throughput becomes almost constant. So, while considering the throughput and utilization ratio hybrid and pipeline topologies are best suited over parallel topology.

REFERENCES

[1] Mohammad Tahghighi et al. "A New Hybrid Topology for Network on Chip" (ICEE), May Edition, 2012.

[2] Danijela Jakimovska et al. "Performance Estimation of Novel 32-bit and 64-bit RISC based Network Processor Cores," (JSAT), May Edition, 2011.

[3] Jing Fu and Olof Hagsand "Designing and Evaluating Network Processor Applications," IEEE 2005.

[4] Jingnan Yao et al. "Optimal Network Processor Topologies for Efficient Packet Process Process Processing," IEEE GLOBECOM, 2005.

[5] P. Crowley et al. "Characterizing processor architectures for programmable network interface,." International Conference on Supercomputing, May 2000.

[6] Ning Weng et al. "Pipelining vs. Multiprocessors– Choosing the Right Network Processor System Topology," University of Massachusetts at Amherst, 2004.

[7] P. Crowley and J.-L. Baer, "A modeling framework for network processor systems," (HPCA-8), Feb 2002.

[8] Kanishka Lahiri et al. "System-Level Performance Analysis for Designing On-Chip Communication Architectures," IEEE TRANSACTIONS, June 2001.

[9] L. Thiele, S. Chakraborty et al. "Design space exploration of network processor architectures," (HPCA-8), Feb 2002.

ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 2, Issue 1, January 2013

[10] Andrew Heppel et al. "An Introduction to Network Processors"(Roke Manor Research),2003.

[11] White Paper "Network Processor Designs for Next-Generation Networking Equipment" (EZChip Technologies), Dec 1999.

[12] Xin Huang and Tilman Wolf "A Methodology for Evaluating Runtime Support in Network Processors"(ANCS),Dec 2006.

AUTHOR BIOGRAPHY

Shuchi Bhagwani is a M.Tech candidate in the Computer Science and Engineering Department at SRCEM Banmore affiliated by the RGPV University Bhopal (M.P.). Her research interests include network processors. She is BE from NRIITM Gwalior affiliated by the RGPV University, Bhopal (M.P.).