ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 2, Issue 1, January 2013

Performance Analysis of Sequential Circuits using reversible logic

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Abstract -This paper presents the introduction of basics reversible logic gates used for reversible operation & one of the applications as Synchronous counter. When we say reversible computing, we mean performing computation in such a way that any previous state of the computation can always be reconstructed given a description of the current state. In recent years, reversible logic has emerged as a promising computing paradigm having application in low power CMOS, quantum computing, nanotechnology, and optical computing. The classical set of gates such as AND, OR, and EXOR are not reversible. In this paper, we have proposed comparison of synchronous & asynchronous counter using Sayem reversible gate. In the comparative analysis we have compared the number of gate, garbage output & power dissipation.

Keywords **– Reversible Logic, Reversible gate, Flip-Flop, Reversible counter, Garbage**.

I. INTRODUCTION

When we say reversible computing, we mean performing computation in such a way that any previous state of the computation can always be reconstructed given a description of the current state. Such a computation is "reversible" since the reconstruction of previous states could be applied to allow progressing backwards through the computer's sequence of states, in a time-reversed fashion. Maintaining the property of reversibility requires that no information about the state of the computer can ever be thrown away. Reversible computation in a system can be performed only when the system consist of reversible gates. Landauer has shown that for irreversible logic computations, each bit of information lost generates kT ln2 joules of heat energy, where k is Boltzmann's constant and T the absolute Temperature at which computation is performed [1]. Bennett showed that kTln2 energy dissipation would not occur, if a computation is carried out in a reversible way [2]. Reversible logic are circuits (gates) that have the same number of inputs and outputs and have one-to-one mappings between input vectors and output vectors; thus the input vector states can be always uniquely reconstructed from the output vector states. A reversible gate with k inputs and k outputs is called a k*k gate. The input vector states can be uniquely reconstructed from the output vector states. A reversible gate named Sayem Gate is 4x4 reversible gates. This gate can be build using reversible combination of Fredkin gate and Feynman gate. T flip flop has been designed using Sayem gate. This T flip flop is used for the design of Synchronous & Asynchronous counter. Implementation has been done using 0.35 micron technology.

II. BASIC REVERSIBLE GATES

A. *Feynman Gate*

Feynman gate is a 2*2 one-through reversible gate shown in Fig. 2. It is called 2*2 gates because it has 2 inputs and 2 outputs. One through gate means that one input variable is also the output. The input double (A, B) associates with its output double (P, Q) as follows. P=A; Q= A ⊕ B [3].

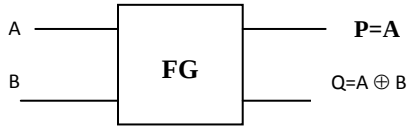

Fig. 1 Feynman gate

ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
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Table I Truth table for Feynman gates

Input		Output	
A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

B. Fredkin Gate

Fredkin gate is a (3*3) conservative reversible gate originally introduced by Petri [3]. It is called 3*3 gates because it has three inputs and three outputs. The input triple (A, B, C) associates with its output triple (P, Q, R) as fallows.

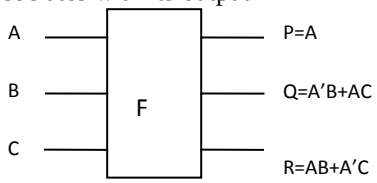

Fig. 2 Fredkin gate

Table II Truth Table for Fredkin gate

Input			Output		
A	*B*	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

C. Toffoli gate

Toffoli Gate (TG) [3] is a 3*3 two-through reversible gate as shown in Fig. 3. In Toffoli Gate, the outputs P and Q are directly generated from inputs A and B respectively by hardwiring. This gate is also suitable for both the forward as well as backward computation.

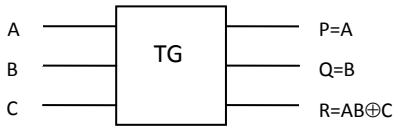

Fig. 3 Toffoli Gate

Table III Truth table for Toffoli gate

Input			Output		
A	*B*	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

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D. Sayem Gate

A reversible gate named Sayem Gate is 4x4 reversible gates. This gate can be build using reversible combination of Fredkin gate and Feynman gate. The block diagram of the gate is shown in Fig. 4. Its corresponding Truth Table is shown in Table 4. From this truth table we can verify that the input and output vectors are unique which satisfies the condition of reversibility. This gate can be used as a two input universal gate means it can perform any two input Boolean function. If we give the 3rd input 0 and 4th input 1 we get NAND of first two inputs at the 4th output which satisfies the universality of a gate in Boolean logic. This operation is shown in Fig 4. With this new reversible SG reversible Latches can be design efficiently.

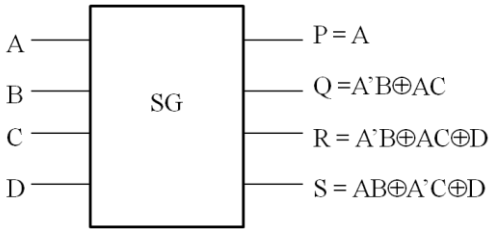

Fig.4 Sayem gate

Table IV Truth table for Sayem gate

Input				Output			
A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	1
0	0	1	0	0	0	0	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	1
0	1	1	1	0	1	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	1
1	0	1	0	0	1	1	0
1	0	1	1	0	1	0	1
1	1	0	0	1	0	0	1
1	1	0	1	1	0	1	0
1	1	1	0	1	1	1	1
1	1	1	1	1	1	0	0

E. Reversible Positive Edge Triggered T Flip-flop

As the name suggests, this flip-flop circuit used to toggle the output when input is high (1) and retains the output when input is low (0), thus it does two operation, it either holds the last state or toggles the output. Essentially, it has a logical symmetry with Controlled NOT kind operation. The reversible realization of T Flip-flop has two SG gates and one Feynman Gate is shown in fig. 5[5].

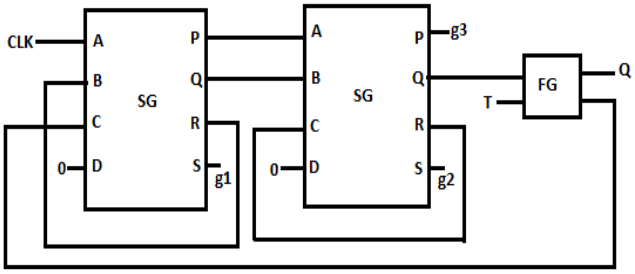

Fig 5: Reversible Positive Edge Triggered T Flip-flop

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III. CMOS IMPLEMENTATION

A. TRANSISTOR IMPLEMENTATION OF SAYEM GATE

Figure 6 shows the Transistor implementation of Sayem gate. Actually the Sayem Gate is the combination of Fredkin Gate (FRG) and Feynman Gate (FG), and so it can simultaneously generate three output functions (from Q, R and S). The output P is taken directly from input A as it is hardwiring. It takes 20 transistors for proposed completely reversible implementation of the Sayem gate. The proposed implementation is suitable for forward as well as backward computation [4].

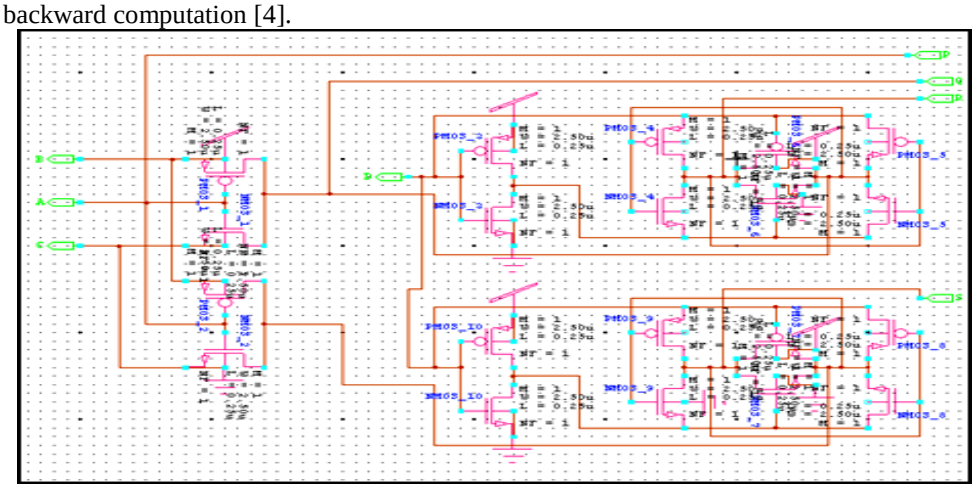

Fig. 6 Transistor implementation of Sayem gate

B. Transistor implementation of four bit Asynchronous up counter

Fig. 7 shows the Transistor implementation of four bit Asynchronous reversible up counter. In a ripple/asynchronous counters, the output transition of one Flip-flop serves as a source for triggering other flip-flops. Two inputs are given to circuit i.e. enable and clock pulses in sequence and we get the four outputs i.e. QA, QB, QC, QD. Here each time we have given the Complemented output to the clock input of T flip-flop. This design is same as conventional design, but we have made only change in reversible T flip-flop in our design. It will count the clock pulses starting from initial value i.e. 0000, 0001, 0010, 0011, 0100 likewise [6].

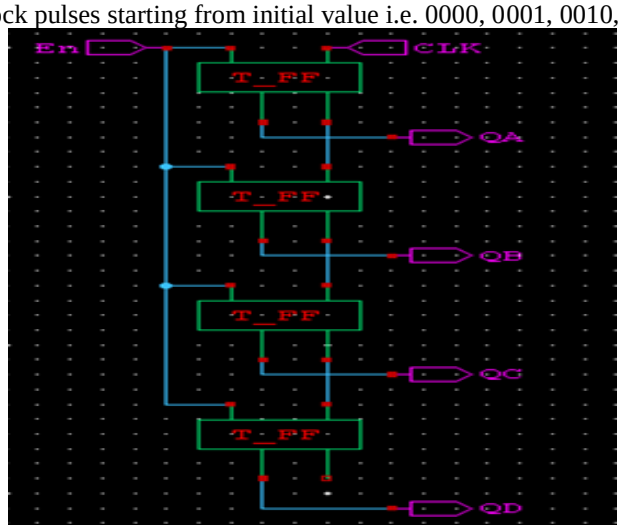

Fig.7 Transistor implementation of four bit Asynchronous up counter

C. Transistor implementation of four bit Asynchronous down counter

Figure 8 shows the Transistor implementation of four bit Asynchronous reversible down counter. Two inputs are given to circuit i.e. enable and clock pulses in sequence and we get the four outputs i.e. QA, QB, QC, QD. This design is same as conventional design, but we have made only change in reversible T flip-flop in our design. It will count the clock pulses starting from initial value i.e.1111, 1110, 1101, 1100, and 1011 likewise

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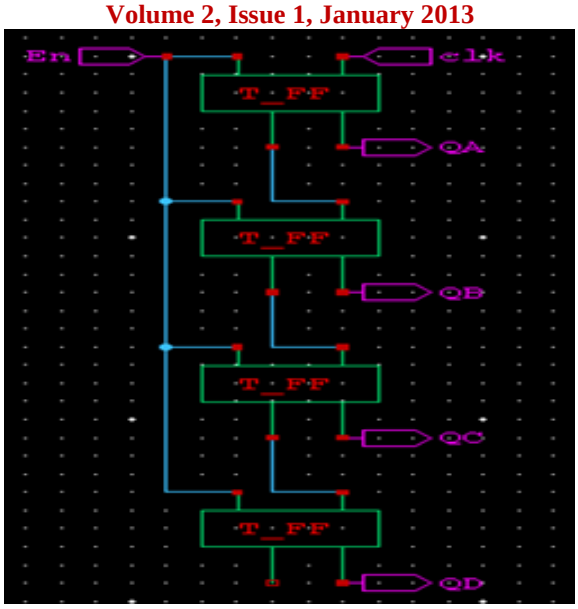

Fig. 8 Transistor implementation of four bit Asynchronous down counter

D. Transistor implementation of four bit Asynchronous bidirectional counter

The reversible design of the asynchronous Up/Down (bidirectional) Counter is shown in Figure 9 The Up/Down operation of this reversible design is controlled by the control input up/down (udb). When this control input is 1 the reversible design operates as an Up counter. When this control input is 0 the reversible design operates as a Down Counter. The proposed reversible counter design contains 19 reversible gates and produces 20 garbage outputs

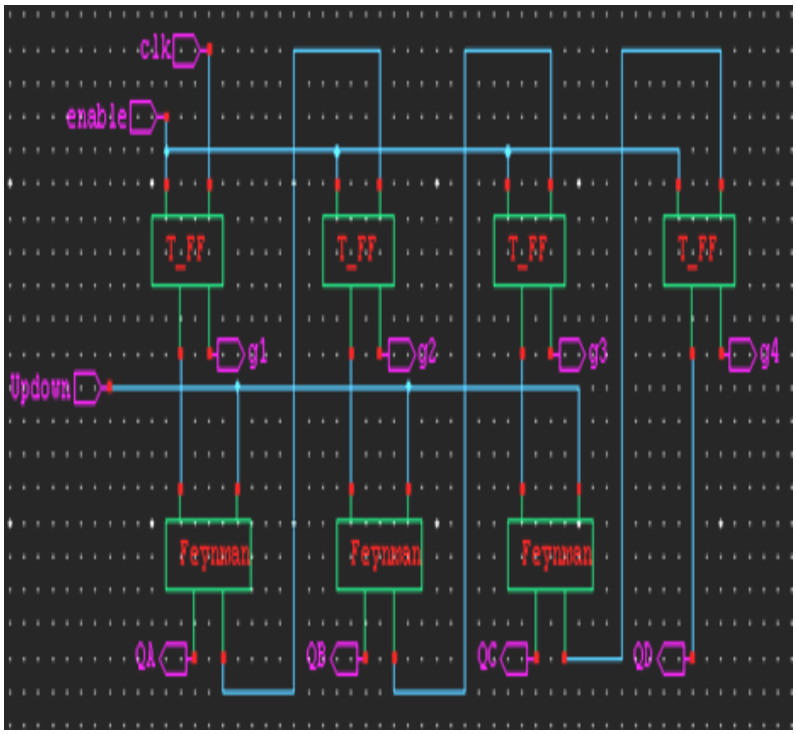

Fig. 9 Transistor implementations of four bit Asynchronous bidirectional counter

E. Transistor implementation of four bit Synchronous up counter

Figure 10 shows the Transistor implementation of four bit Synchronous reversible up counter. Enable and clock inputs are given to the circuit. All clock terminal of each T flip-flop are connected to common clock input. We have used AND properties of Fredkin gate to combine the inputs and fed to T input of T flip-flop. We have four outputs i.e. QA, QB, QC, QD. Here we have used four T flip-flop and six Fredkin gate to implement up counter.

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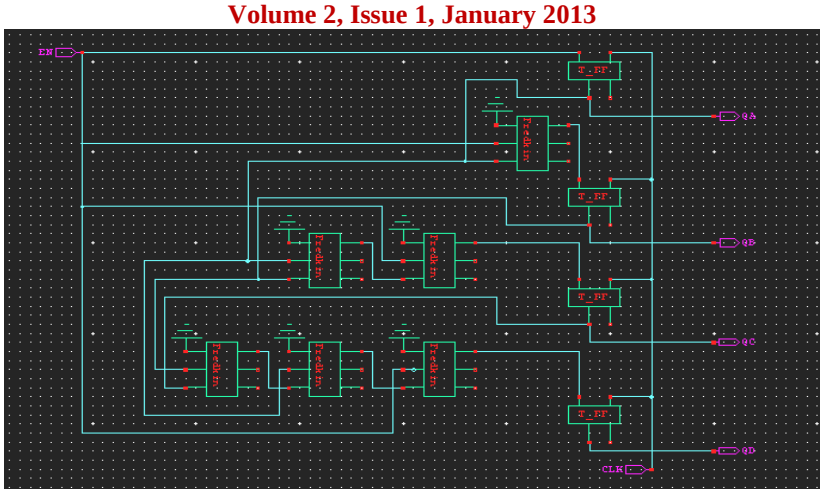

Fig.10 Transistor implementation of four bit Synchronous up counter

F. Transistor implementation of four bit Synchronous down counter

Figure 11 shows the Transistor implementation of four bit Synchronous reversible up counter. The Vcc input is given to first T flip-flop. All clock terminal of each T flip-flop are connected to common clock input. We have four outputs i.e. QA, QB, QC, QD. Here we have used four T flip-flop and three Fredkin gate to implement down counter.

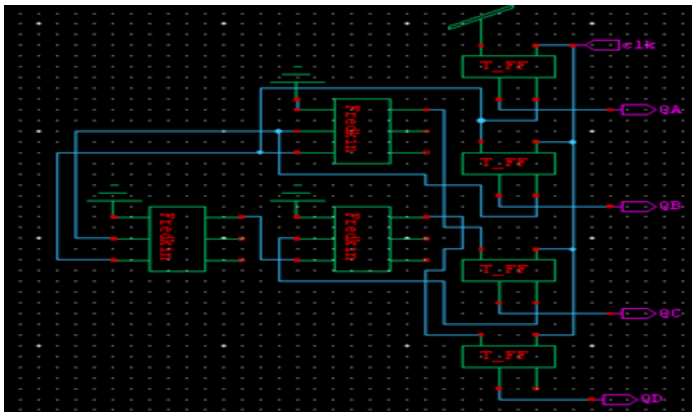

Fig.11 Transistor implementation of four bit Synchronous down counter

G. Transistor implementation of four bit Synchronous bidirectional counter

The reversible design of the Synchronous Up/Down (bidirectional) Counter is shown in Figure 4.11. The Up/Down operation of this reversible design is controlled by the control input up/down. When this control input is 1 the reversible design operates as an Up counter. When this control input is 0 the reversible design operates as a Down Counter. The proposed reversible counter design contains 14 reversible gates, produces 10 garbage outputs

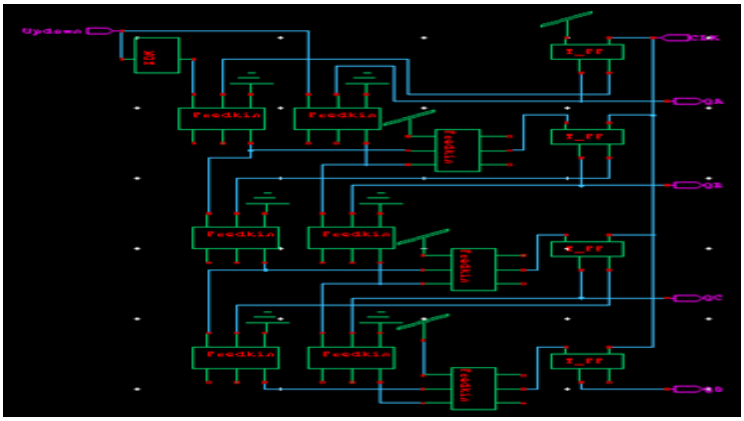

Fig. 12 Transistor implementation of four bit Synchronous bidirectional counters

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IV. SIMULATION RESULTS

1. Simulation result of four bit reversible asynchronous up counter

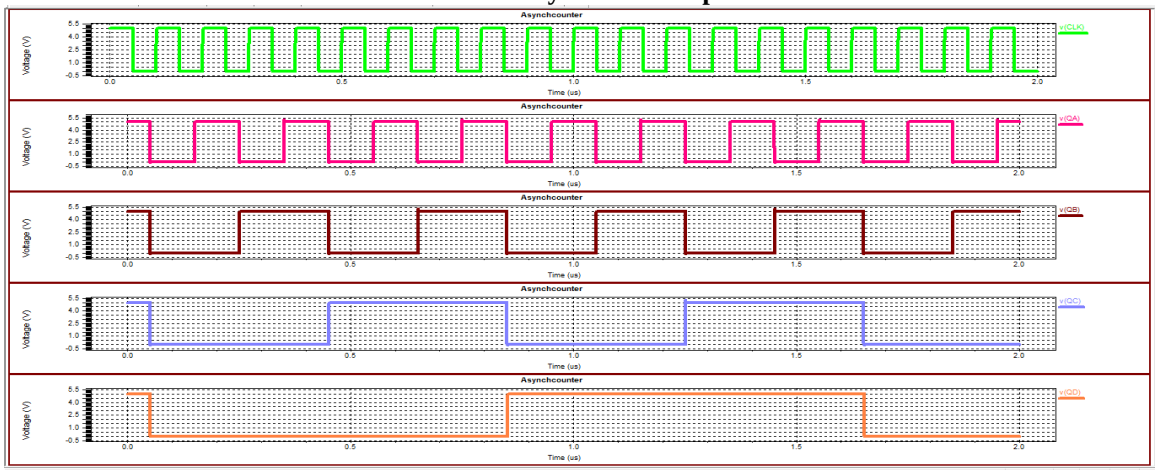

Fig 13 simulation result of four bit reversible asynchronous up counter

Measurement result summary avg_power = 1.1357e-004

2. Simulation result of four bit reversible asynchronous down counter

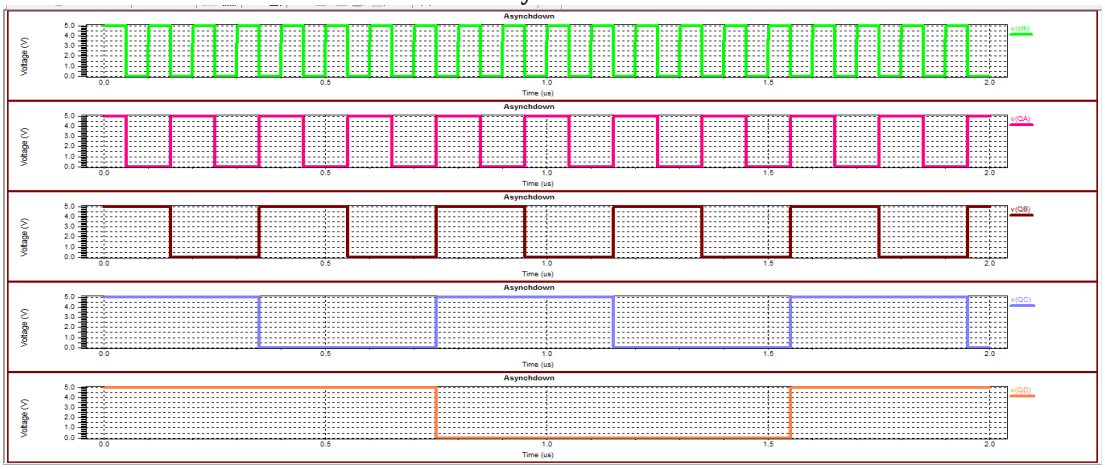

Fig 14 simulation result of four bit reversible asynchronous down counter

Measurement result summary avg_power = 2.0336e-003

3. Simulation result of four bit reversible asynchronous bidirectional counter

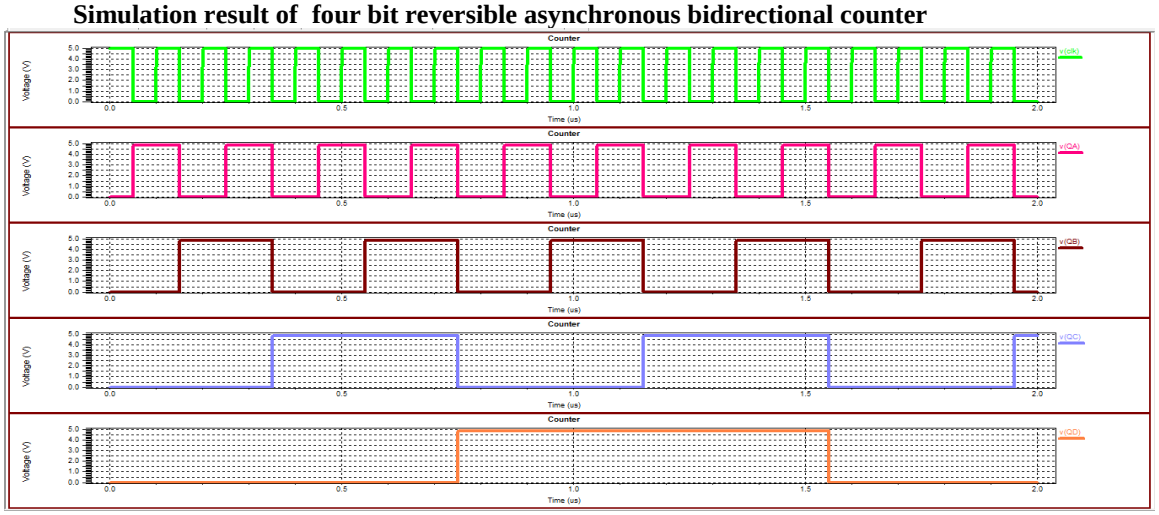

Fig 15 simulation result of four bit reversible asynchronous bidirectional counter

Measurement result summary avg_power = 7.2503e-003

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4. Simulation result of four bit reversible synchronous up counter

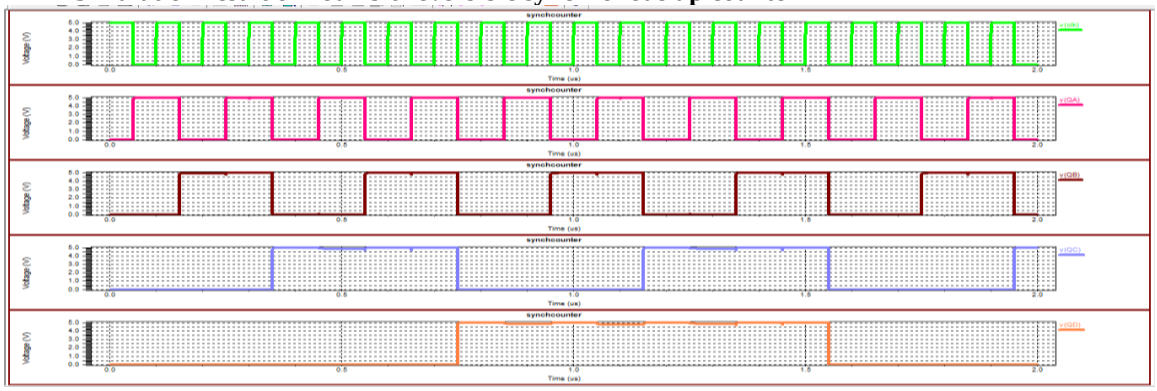


Fig 16 simulation result of four bit reversible synchronous up counter

Measurement result summary avg_power = 2.3580e-003

5. Simulation result of four bit reversible synchronous down counter

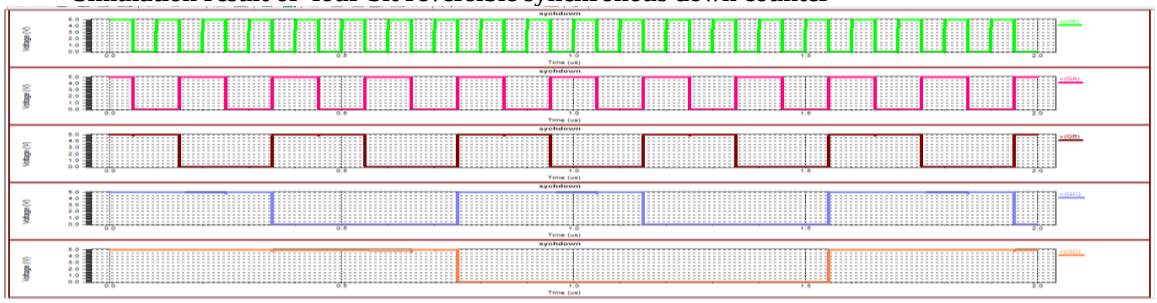
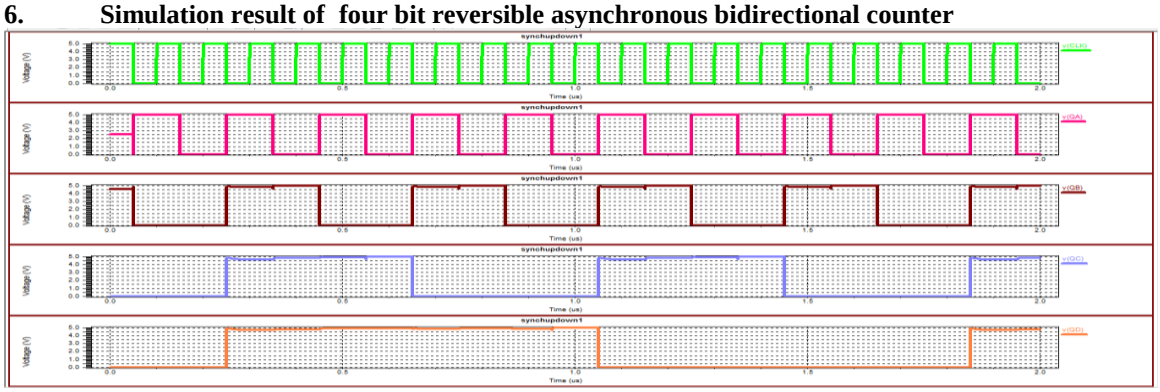


Fig 17 simulation result of four bit reversible synchronous down counter

Measurement result summary avg_power = 1.8667e-003

6. Simulation result of four bit reversible asynchronous bidirectional counter



V. COMPARATIVE ANALYSIS

Table V Comparative result analysis of different counter

Proposed design	No. of Gate	Garbage O/P	Power dissipation
Asynchronous up counter	16	17	1.1357e-004
Asynchronous down counter	16	17	2.0336e-003
Asynchronous bidirectional	19	20	7.2503e-003
Synchronous up counter	22	32	2.3580e-003

ISSN: 2319-5967
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Synchronous down counter	19	23	1.8667e-003
Synchronous bidirectional counter	25	35	5.3435e-003

VI. CONCLUSION

Table 5 shows comparison of different sequential circuit. As this is new approach to sequential circuit design using reversible gate. We made attempt to compare our design of different sequential circuit with respect to power dissipation factor. We observed that Synchronous up/down counter has less power dissipation as compared to the Asynchronous up/down counter.

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