



ISSN: 2319-5967

ISO 9001:2008 Certified

International Journal of Engineering Science and Innovative Technology (IJESIT)

Volume 1, Issue 2, November 2012

An Efficient Architecture for Multi-Level Lifting 2-D DWT

P.Rajesh

S.Srikanth

V.Muralidharan

Assistant Professor

Assistant Professor

Assistant Professor

SNS College of Technology

SNS College of Technology

Christ the King Engineering College

Abstract- A efficient VLSI based architecture is proposed in this paper for implementation Discrete Wavelet Transform (DWT) of 5/3 filter. The proposed architecture includes transforms modules, a RAM and bus interfaces. This architecture works in non separable fashion using a serial-parallel filter with distributed control to compute all the DWT (1D-DWT and 2D-DWT) resolution levels.

Keywords- Discrete Wavelet Transform, Lifting Scheme, 5/3 Filter

I. INTRODUCTION

2-D DWT has evolved as essential part of modern compression system such as JPEG 2000. This is because the DWT can decompose the signals into different sub bands with both time and frequency information and facilitate to arrive a high compression ratio [1]. In addition ,a wavelet based compression system, not only presents superior compression performance over DCT ,but provides four dimension of scalabilities resolution, distortion, spatial and color, which are very difficult to achieve in DCT based compression system. In a compression system, the function of DWT is to decorrelate the original image pixels prior to compression step such that they can be amenable to compression. Therefore many famous coders have been proposed to effectively compress images or frames processed via DWT. The computation of DWT can be done either by convolution based scheme or Lifting based scheme. The lifting scheme of computation of DWT has, however, become more popular over the convolution-based scheme for its lower computational complexity [2] .The main feature of the lifting-based DWT scheme is to break up the high pass and low-pass filters into a sequence of upper and lower triangular matrices and covert the filter implementation into banded matrix multiplications. Such a scheme has several advantages, including “in-place” computation of DWT, integer-to integer wavelet transform, symmetric forward and inverse transform. The popularity of lifting-based DWT has triggered the development of several architectures in recent years. The architecture lifting-based 2D-DWT developed in [3] has regular data flow and low control complexity, and achieves 100% hardware utilization. The other architecture was based propriety of perfect reconstruction of filter bank developed in [4]. Many architectures of DWT were proposed in literature combined lossy and lossless transform like [5],the aim of this brief is to embed the 5/3 wavelet computation into the 9/7, in order to exploit as much as possible the 5/3 results to achieve the 9/7 ones, with a reduced number of adders compared to other solutions. In [6] the proposed architecture can be reconfigured for 5/3 and 9/7 wavelet transforms. This reduces significantly the required numbers of the multipliers, adders and registers, as well as the amount of accessing external memory, and leads to decrease efficiently the hardware cost and power consumption of design. In [7] the architecture for 1D-DWT principle can be extended to architectures for separable 2D-DWT like the one developed in [8],[9].

The remaining paper is organized in the following manner: the next section provides a brief overview of the lifting scheme DWT algorithm. In the section 3, the proposed architecture system and its internal components are described in details. Comparisons results with other architectures related works are also presented in section 4.Finally, conclusions are discussed in section 5.

II. LIFTING BASED DWT

In traditional convolution (filtering) based approach for computation of the forward DWT, the input signal (x) is filtered separately by a low-pass filter (\tilde{h}) and a high-pass filter (\tilde{g}). The two output streams are then sub-sampled by simply dropping the alternate output samples in each stream to produce the low-pass (y_L) and high-pass (y_H) sub-band outputs.

The lifting-based DWT has many advantages over the convolution based approach. Some of them are as follows.

- Lifting-based DWT typically requires less computation (up to 50%) compared to the convolution based approach. However the savings depends upon the length of the filters.



ISSN: 2319-5967

ISO 9001:2008 Certified

International Journal of Engineering Science and Innovative Technology (IJESIT)

Volume 1, Issue 2, November 2012

- During the lifting implementation, no extra memory buffer is required because of the in-place Computation feature of lifting. This is particularly suitable for hardware implementation with limited On-chip memory.
- The lifting based approach offers integer to integer transformation suitable for lossless image Compression.
- In lossless transformation mode, the boundary extension of the input data can be avoided because the original input can be exactly reconstructed by integer to integer lifting transformation.

The advantage of lifting scheme is the forward and inverse transform was obtained from the same architecture. The inverse goes from right to the left, by inverting the coefficients of normalized and changes the sign positive to negative.

The polyphase representation of discrete filter $h(n)$ is defined as

$$h(z) = h_e(z) + Z^{-1}h_o(z)$$

Where $h_e(z)$ and $h_o(z)$ are respectively obtained from the even and odd zeta transform respectively. If we represent $h(z)$ and $g(z)$ the low pass and high pass coefficients of the synthesis filter respectively, the polyphase matrix written as:

$$p(z) = \begin{bmatrix} h_e(z) & g_e(z) \\ h_o(z) & g_o(z) \end{bmatrix}$$

The filters $h_e(z)$, $h_o(z)$, $g_e(z)$ and $g_o(z)$ are Laurent polynomials, as the set of all polynomials exhibits a commutative ring structure, within which polynomial division with remainder is possible, long division between two Laurent polynomials is not a unique operation. In Euclidean algorithm decomposition can be used, the polyphase $p(z)$ is finally obtained as:

$$p(z) = \prod_{i=1}^m \begin{bmatrix} 1 & s_i(z) \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ t_i(z) & 1 \end{bmatrix} \begin{bmatrix} k & 0 \\ 0 & \frac{1}{k} \end{bmatrix}$$

Where $s_i(z)$ and $t_i(z)$ primary lifting and dual lifting steps filters respectively, k is a constant of normalization at low and high coefficients filters.

The 5/3 wavelet filter transform is more suitable lossless data compression adopted in JPEG2000 and 9/7 filter is used in JPEG2000 for lossy compression data. The 5/3 filter has one prediction and one up-dating compared to two predictions and two up-dating for 9/7 filter. The following steps are necessary to get their wavelet coefficients as the following tapes for 5/3 filter: Split the input signal into coefficients at odd and even positions. Perform a predict step, followed by up-dating step.

$$a(2n) = x(2n) + \left[\frac{d(2n-1) + d(2n+1) + 2}{4} \right]$$

These equations are illustrate and presented in the Fig.1 for direct lifting scheme of bi-orthogonal 5/3 filter, where the constant k is equal unit.

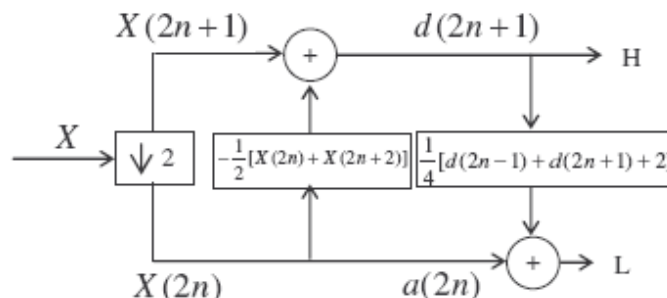


Fig.1 Lifting Scheme Decomposition of 5/3 Filter



ISSN: 2319-5967

ISO 9001:2008 Certified

International Journal of Engineering Science and Innovative Technology (IJESIT)

Volume 1, Issue 2, November 2012

The lifting based implementation of two levels 2D-DWT may be computed using filter banks as shown in Fig.2. The input samples X(n) are passed through two stages of analysis filters. They are first processed by low-pass (h(n)) and high-pass (g(n)) horizontal filters and are sub sampled by two. Subsequently, the outputs (L1, H1) are processed by low-pass and high-pass vertical filter. Note that: L1, H1 are the outputs of 1D-DWT; LL1, LH1, HL1 and HH1 one-level decomposition of 2D-DWT.

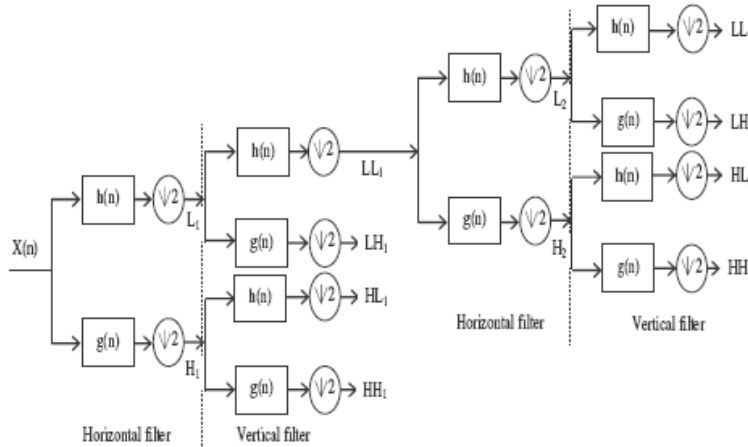


Fig.2 Sub band Decomposition for Two-Level 2D-DWT

III. OUR PROCESSOR DESIGN AND IMPLEMENTATION

This section presents the architecture design of our programmable DWT processor. This processor can perform the 1D-DWT and 2D-DWT with multi-levels decomposition upon in the user needs.

A. Components of Our Processor Design

A block based top-level implementation of our proposed processor is shown in Fig.4. The proposed system supports seven blocks. The architecture shown one level decomposition but it is reconfigurable for the multi-levels decomposition in our need. In this Fig.3, basic units of the architecture system are shown. The following units are:

- A Bus Interface Unit has been integrated in order to achieve communication efficiently with the external environment.
- The Control Unit is designed to control the data flow in the design, as well as the data transfer between the interface Unit, the Processing Computation Unit and the RAM Unit. A FSM is used for this purpose. During initialization phase, the user with the appropriate write commands selects the decomposition DWT type (1D-DWT, 2D-DWT and with multi-levels decompositions). The Control Unit coordinates all system operations and processes. After the initialization phase, the control unit is totally responsible for the system operation. The control unit manages the operation of 2D-DWT serial-parallel even-odd filter (Fig.2). It controls the data input, the synchronization of the operations, and the data output.
- The block processing elements: each of them contains a multiplier and an adder. Every five clock cycle one processing element is generated for band H and band L transformed pixels. The block has the higher computation task of our architecture.
- The blocks processing band H and band L are needed in the case of 2D-DWT and multi levels decompositions. These blocks used the arithmetic logic operation of details and approximation coefficients respectively. The RAM block is used for storage of the L and H coefficients for the next transformations types (2D-DWT or multi levels decomposition).The output accumulator is the final block in the architecture. This produces output data by storing the results of different transformations; it is generated under the control of a synchronous available signal.

B. Working Procedures

Our design presents various transformations like the 1D-DWT, 2D-DWT and multi level decomposition of DWT. The decomposition scheme is level by level and described as follows:

The 2D-DWT, in first-level decomposition, the bus interface unit selects data (pixels) from input image. The transform module (Processing, processing band H and processing band L) decomposes to the four sub-bands LL1, LH1, HL1 and HH1, and saves LL1 band to the RAM module. After finishing the first level decomposition, the controller unit selects data from RAM module. The LL1 band is then sent to the module

transform to perform the second level decomposition. The transform module decomposes the LL1 band to the four sub-bands LL2, LH2, HL2 and HH2, and saves LL2 band to the RAM module for next level decomposition. This procedure repeats until the desired N level (last level) decomposition is finished.

The 1D-DWT, in first-level decomposition the bus interface unit selects data (pixels) from input image. The transform module (Processing) decomposes to the two sub-bands L1 and H1 and saves L1 band to the RAM module. In second level the controller unit selects data (band L1) from RAM module. The module transform (processing band L) decompose the band L1 to the two sub-bands L2 and H2 and save band L2 to the RAM module for next level decomposition. They blocks of process are shown in Fig.4.

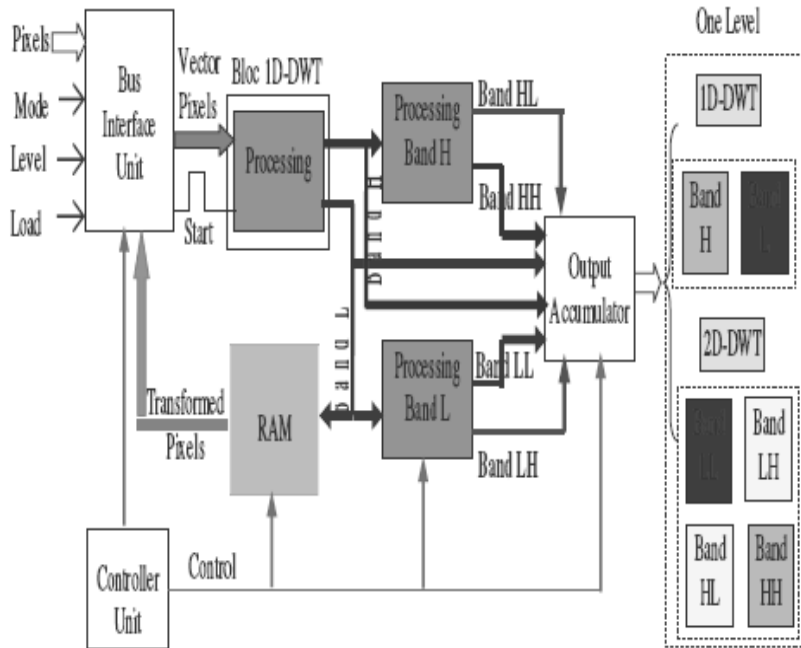


Fig.3 Our Direct DWT Architecture Design

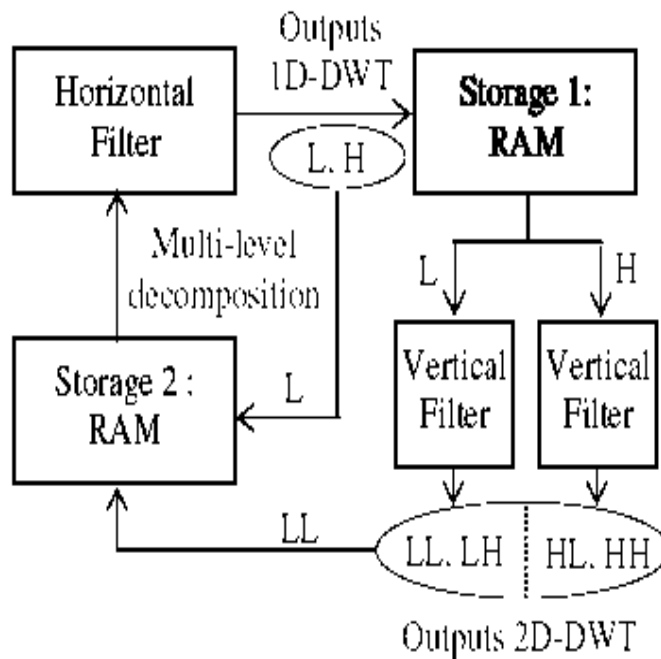


Fig.4 Serial-Parallel Module Transforms



ISSN: 2319-5967

ISO 9001:2008 Certified

International Journal of Engineering Science and Innovative Technology (IJESIT)

Volume 1, Issue 2, November 2012

Table I Performance and Comparisons 2D-DWT of our Architecture

Parameters	Our Architecture	RFA [7] modified	Architecture [10]	Architecture [2]	Architecture (BB) [12]
Filter	5/3	5/3(or)9/7	5/3(or)9/7	9/7	5/3
Implementation	Lifting	N.A	N.A	Lifting	Lifting
Computation time	2.36 ms	5.88 ms	N.A	N.A	N.A
Number Slices	1835	2554	4720	7726	2646
Frequency	108 Mhz	45Mhz	75Mhz	66.8Mhz	116.4Mhz
Hardware Efficiency	100%	65%	69%	100%	100%
Control complexity	simple	complex	complex	Complex	complex

IV.PERFORMANCES AND COMPARISONS

In this section, we present the different performance of our architecture serial-parallel and compare the results with the Recursive Pyramid Algorithm (RFA), modified in [7] and, with Pyramid Algorithm Analysis developed in [10], which have the same device of our architecture. We compare our architecture with other different device like the recent work of implementation of 5/3 lifting architectures Based-Block (BB) implementation in FPGAs developed in [12], and architecture developed in [2] similar in our architecture. Therefore, this performance comparison of different architectures is presented in Table I.

Our architecture uses serial input of read data (pixels of image) and parallel processing of different pixels. Therefore we compare our architecture with different topologies of 2D-DWT architectures. Our architecture is efficient and flexible like the one parallel architecture developed in [12]. Table I, compares the hardware performance of the implemented architecture. This table presents comparative results of our architecture, in terms of frequency, number of FPGA slices, computing time, hardware efficiency and control complexity with others architectures.

V.CONCLUSION

In this work we have proposed flexible architecture for the implementation of multi-level decomposition DWT (1D and 2D) by 5/3 filter. Our architecture has been correctly verified as 100% hardware utilization, fast computing time and low control complexity. Our works are suitable for the next generation image/video compression using multilevel decomposition DWT.

REFERENCES

- [1] M.A. Suhail and M.S. Obeidat "One digital Watermarking in JPEG 2000" Electronics, Circuits and Systems. The 8th IEEE International Conference on Volume 2, ICECS 2001, Pages: 871- 874.
- [2] T. Acharya and C. Chakrabarti "A Survey Lifting-based Discrete Wavelet Transform Architectures" Journal of VLSI Signal Processing 42, 321-339, 13 February 2006.
- [3] S. Barua, J.E. Charletta, K.A. Kotteri and A.E. Bell "An efficient architecture for lifting-based two-dimensional discrete wavelet transforms" Integration, the VLSI Journal 38, 341-352, 21 July 2004.
- [4] K. A. Kotteri, A. E. Bell and J. E. Carletta "Design of Multiplier less, High-Performance, Wavelet Filter Banks With Image Compression Applications" IEEE Transactions Circuits and Systems – I: Regular Papers, vol. 51, N° 3, March 2004.
- [5] M. Martina and G. Masera "Multiplier less, Folded 9/7-5/3 Wavelet VLSI Architecture" IEEE Transactions on Circuits and Systems-II:Express Briefs, vol.54 N°. 9, September 2007.
- [6] X. Chengyi, T. Jinwen and L. Jian " Low complexity reconfigurable architecture for the 5/3 and 9/7 discrete wavelet transform" Journal of Systems Engineering and Electronics vol. 17 N° 2, pp. 303-308, 2006.
- [7] R.J.C. Palero, R.G. Gironés and A.S. Cortes "A Novel FPGA Architecture of a 2-D Wavelet Transform" Journal of VLSI Signal Processing 42, 273-284, August 4, 2005.
- [8] P.C. Wu and L.G. Chen "An efficient architecture for two-dimensional discrete wavelet transform" IEEE Transaction on Circuit and Systems and Systems for Video Technology, Volume 11, N° 4, April 2001, Pages 536-545.
- [9] Dhaha Dia, Medien Zeghid, Taoufik Saidani, Mohamed Atri, Belgacem Bouallegue, Mohsen Machhout and Rached Tourki, " Multi-level Discrete Wavelet Transform Architecture Design" Proceedings of the World Congress on Engineering 2009 Vol I WCE 2009, July 1 - 3, 2009, London, U.K.



ISSN: 2319-5967

ISO 9001:2008 Certified

International Journal of Engineering Science and Innovative Technology (IJESIT)

Volume 1, Issue 2, November 2012

- [10] A. Benkrid, D. Crookes and K. Benkrid “Design and Implementation of Generic 2-D Biorthogonal Discrete Wavelet Transform on an FPGA” IEEE, Proceedings of the 9th Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 2001.
- [11] A. Pande, J. Zambreno “Design and analysis of efficient reconfigurable wavelet filter” IEEE of International Conference on Volume, issue 18-20, May 2008, Pages: 327-332.
- [12] M.E. Angelopoulos, P.Y.K. Cheung, K. Masselos and Y. Andreopoulos “Implementation and comparison of 5/3 Lifting 2D DWT Computation Schedules on FPGAs” Journal of Signal Systems 51, 3-21, 2008.

AUTHOR BIOGRAPHY



Rajesh.P received the B.E degree from P.S.R Engineering College, Tamilnadu, India in 2009 and received M.E degree from S.N.S College of technology, Coimbatore, Tamilnadu, India in 2012. He already published one journal related to adders and also attend many international conferences. Now his current research topic is focused on VLSI Design and ASIC Design.



Srikanth.S received his B.E degree in electronics and communication engineering from S.N.S College of technology, Coimbatore and also received M.E degree from Sri Ramakrishna Engineering College; Coimbatore. He already published one journal related to VLSI Design. His area of interest is VLSI signal processing and Computer Architecture.



Muralidharan.V received the B.E degree from maharaja prithvi engineering, Tamilnadu in 2010 and received M.E degree from Sri Ramakrishna Engineering College, Coimbatore, and Tamilnadu, India in 2012. He already published two journals related to adders and also attend many international conferences. His current research topic is focused on VLSI Design.