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Lifting Based 2D DWT Processor for Image Compression

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Abstract *- Digital images play an important role both in daily life applications as well as in areas of research and technology. Due to the increasing traffic caused by multimedia information and digitized form of representation of images; image compression has become a necessity. Wavelet transform has demonstrated excellent image compression performance. New algorithms based on Lifting style implementation of wavelet transforms have been presented in this paper. The original image is transformed using adaptive lifting based Wavelet transforms and it is compressed. This paper presents a high speed and area efficient DWT processor based design for Image Compression applications. The suitability of the 2D Discrete Wavelet Transform (DWT) as a tool in image and video compression is nowadays indisputable. In this proposed design, pipelined partially serial architecture has been used to enhance the speed along with optimal utilization; the architecture consists of two row processors, two column processors, and two memory modules. Each processor contains two adders, one multiplier, and one shifter. The precision of the multipliers and adders has been determined using simulation. The result comparison has shown an improvement in speed. In this compression techniques uses lifting scheme with DWT, blocking artifact and bad subjective quality are improved than in convolution method using DWT. Conventional lifting-based architectures require fewer arithmetic operations compared to the convolution-based approach for DWT. In addition to this and for the reason to preserve proper precision, intermediate variables widths are larger in lifting based computing. As a result, the lifting multiplier and adder delays are longer than the convolution ones. The implementations are fully parameterized with respect to the size of the input image and the number of decomposition levels. The main feature of the lifting based DWT scheme is to break up the high pass and low pass filters into a sequence of upper and lower triangular matrices and convert the filter implementation into banded matrix multiplications [1], [2]. Such a scheme has several advantages, including "in-place" computation of the DWT, integer-to-integer wavelet transform (IWT), symmetric forward and inverse transform, etc. The outputs generated by the row and column processors are stored in memory modules. The memory modules are divided into multiple banks to accommodate high computational bandwidth requirements. The lifting-based DWT architecture consisting of four processor architecture can perform transforms with one or two lifting steps one level at a time. Furthermore, the data path is pipelined, and the clock period is determined by the memory access time of performing filters with one lifting step, i.e., one predict and one update step [10]. The outputs are generated in an interleaved fashion.*

Keywords - **DWT, Lifting Scheme, DWT Processor.**

I. INTRODUCTION

With the increasing use of multimedia technologies, image compression requires higher performance. To address needs and requirements of multimedia and internet applications, many efficient image compression techniques, with considerably different features have been developed [1].The two-dimensional Discrete Wavelet Transform (2D DWT) is nowadays established as a key operation in image processing. In the area of image compression, the 2D DWT has clearly prevailed against its predecessor, the 2D Discrete Cosine Transform. A lifting stage is comprised of the three steps namely Split, Predict, and Update. The lifting scheme is an efficient tool for constructing second generation wavelets and has advantages such as faster implementation, fully in place calculation, perfect reconstruction with low Memory and low computational complexity. This is mainly because it achieves higher Compression ratios, due to the sub band decomposition it involves, while it eliminates the `blocking' artifacts that deprive the reconstructed image of the desired smoothness and continuity. The high algorithmic performance of the 2D DWT in image compression justifies its use as the kernel of both the JPEG-2000 still image compression standard.

A. Discrete Wavelet Transform

DWT can decompose the input samples in multiresolution. The implementation of the discrete wavelet transform is based on the filter banks, where G and H denote a high-pass filter and a low-pass-filter, respectively. After each filtering, the number of the output samples is decimated by a factor of 2. The samples generated by the high pass filters are completely decomposed; meanwhile, the other samples generated by the low pass filters are applied to the next-level computation or further decomposition.

B.Lifting-Based DWT

The lifting scheme is a new algorithm proposed for the implementation of the wavelet transforms [2]. It can reduce the computational complexity of DWT involved with the convolution implementation. Furthermore, the extra memory required to store the results of the convolution can also be reduced by in place computation of the wavelet coefficient with the lifting scheme. Lifting wavelet transform as its advantages over the ordinary

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wavelet transform by way of reduction in memory required for its implementation. The basic principle of the lifting scheme is to factorize the poly phase matrix of a wavelet filter into a sequence of alternating upper and lower triangular matrices and a diagonal matrix [1], [2]. This leads to the wavelet implementation by means of banded-matrix multiplications. Let h(z) and g(z) be the low pass and high pass analysis filters, and let h (z) and g (z) be the low pass and high pass synthesis filters. The corresponding poly phase matrices are defined as

$$\tilde{P}_1(Z) = \begin{bmatrix} k & 0 \\ 0 & \frac{1}{k} \end{bmatrix} \prod_{i=1}^{m} \begin{bmatrix} 1 & s_i(z) \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ t_i(z) & 1 \end{bmatrix} \quad (1)$$

$$\tilde{P}_2(Z) = \begin{bmatrix} k & 0 \\ 0 & \frac{1}{k} \end{bmatrix} \prod_{i=1}^{m} \begin{bmatrix} 1 & 0 \\ t_i(z) & 1 \end{bmatrix} \begin{bmatrix} 1 & s_i(z) \\ 0 & 1 \end{bmatrix} \quad (2)$$

Where k is a constant, $ti_{(z)}$ and $si_{(z)}$ are denoted as primary lifting and dual lifting polynomial respectively and m represents the total lifting steps required. The two types of lifting schemes are shown in Figure 1, which corresponds to the Factorization consists of three steps.

- Predict step, where the even samples are multiplied by the time domain equivalent of t (z) and are added to the odd samples,
- Update step, where updated odd samples are multiplied, by the time domain equivalent of s (z) and are added to the even samples,
- Scaling step, where the even samples are multiplied by 1/k and odd samples by k.

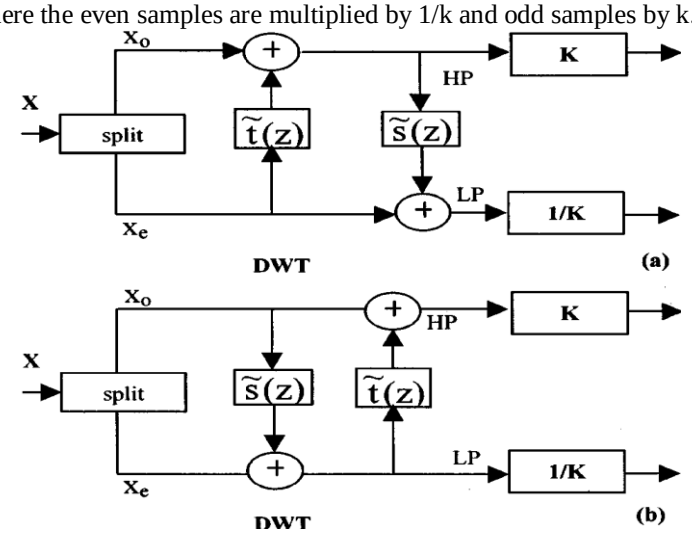

Fig 1. Lifting Schemes. (a) Scheme 1. (b) Scheme 2.

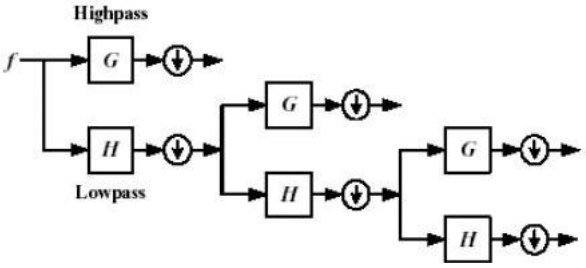

Fig 2. 2-D for Discrete Wavelet Transforms

C. Proposed VLSI Architecture

To perform the DWT, the architecture reads in the block of data, carries out the transform, and outputs the LH, HL, and HH data at each level of decomposition. The LL data is used for the next level of decomposition. At the end of the inverse Transform, the LL values of the next higher level are obtained. The transform values of the three sub bands (LH, HL, and HH) are read in, and the DWT is carried out on the new data set. The architecture, as shown in Fig. 2, consists of a row module (two row processors RP1 and RP2 along with a register file REG1), a column module (two column processors CP1, CP2 and a register file REG2), and two mem0ry modules (MEM1, MEM2).

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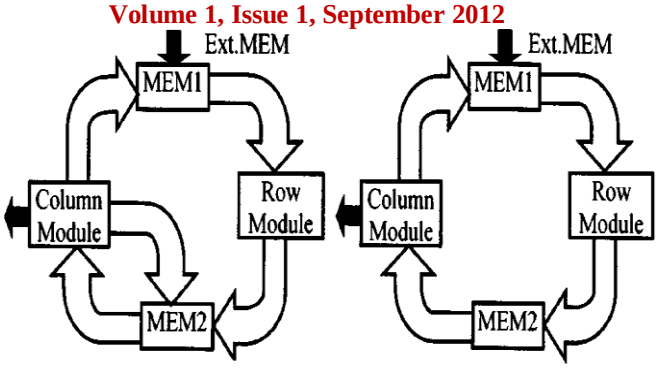

a) b)

Fig 3. A) Block Diagram of the Proposed Architecture B) Data Flow for 2M Filters

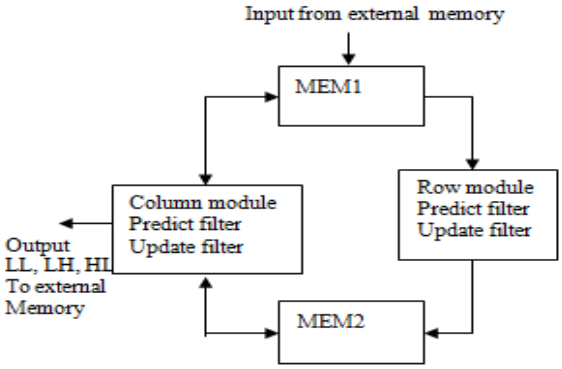

Fig 4. Overview of Lifting Based 2D DWT Architecture

In the 2 case (i.e., when lifting is implemented by two factorization matrices), processors RP1 and RP2 read the data from MEM1, perform the DWT along the rows, and write the data into MEM2. Processor CP1 reads the data from MEM2, performs the column wise DWT along alternate rows, and writes the HH and LH sub bands into MEM2 and Processor CP2 reads the data from MEM2, performs the column-wise DWT along the rows on which the CP1 did not work, and writes LL sub-band to MEM1 and HL sub-band to external memory the data Flow is shown in figure 3.

II. JPEG2000 ALGORITHM

Division of the image into rectangular, non-overlapping tiles [1],[2],[4]. Tiling of components with different sub-sampling factors with respect to a high-resolution grid. Maintaining the size of each tile to be the same, with the exception of tiles around the border (all four sides) of the image. Conversion of the input series into high-pass & low-pass wavelet coefficient series (of length n/2 each) using DWT. The high-pass & low-pass wavelet coeff. Series are given by, [1], [2], [3]:

$$H_i = \sum_{m=0}^{k-1} x_{2i-m} . s_m(z)$$

$$L_i = \sum_{m=0}^{k-1} x_{2i-m} . t_m(z)$$

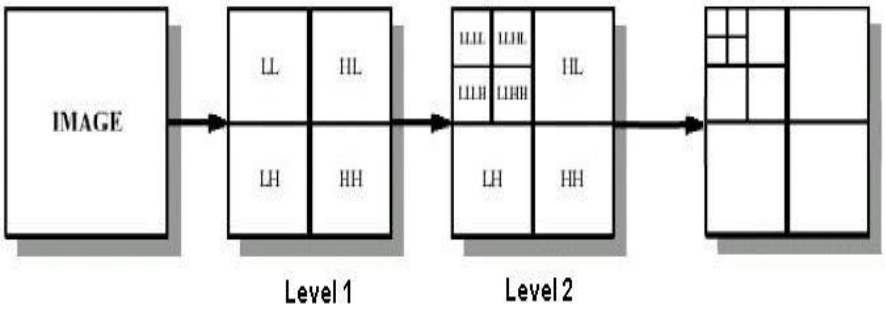

Fig 5. Multi Level Decomposition

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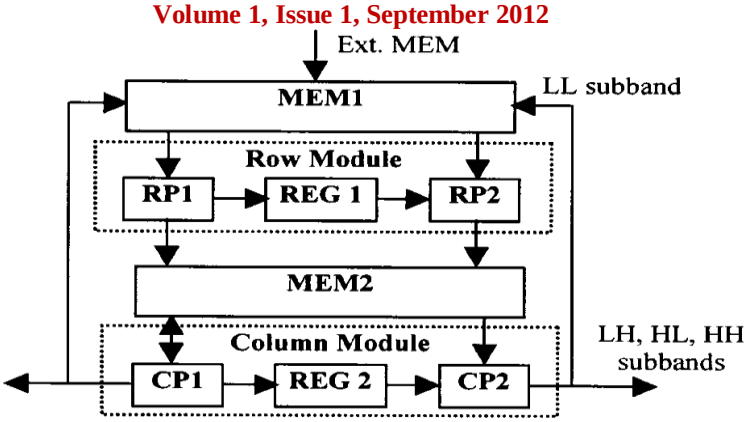
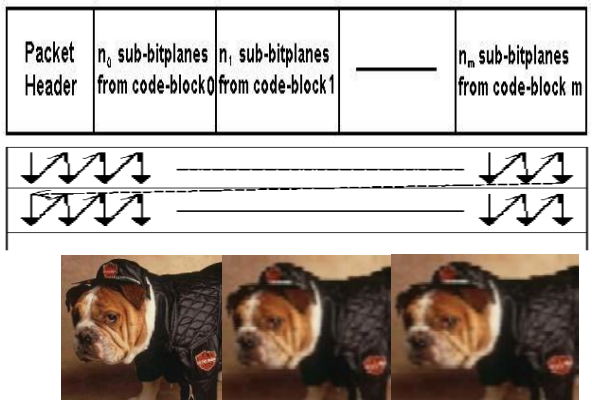


Fig 6. Multi Level Decomposition

Uniform scalar quantization of the wavelet coefficient employing a fixed dead-zone about the origin. Division of the magnitude of each coeff. by a quantization step size and rounding down. Division of each sub-band into regular non-overlapping rectangles by "packet partition". Three spatially consistent rectangles (one from each sub-band) comprise a packet partition location. Code-blocks obtained by dividing each packet partition location into regular non-overlapping rectangles. Entropy coding carried out as context-dependent, binary, arithmetic coding of bit planes. Collection of each code-block in a packet partition location to form the body of a "packet." JPEG 2000 provides protective image security. It provides improved low bit-rate compression performance & provides transmission in noisy environments. It gives improved continuous-tone and bi-level compression of larger images.

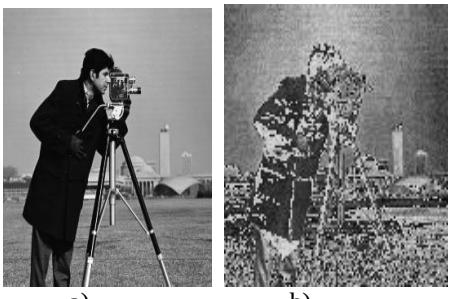


a) b) c)

Fig 7. a) Original Bitmap b) JPEG (DCT) c) JPEG-2000 (DWT) Image (43:1 compression ratio)

III. RESULTS

We have applied the adaptive prediction algorithms to 256×256 8 bit images. The image for testing is the famous Lena with block size of 64×64. With the width of the data bus being 8 bits, the function and logic simulation are carried out on the platform. For smooth images like Lena, 9/7 transform gives much better results.



a) b)

Fig 8. A) Original Image B) 1/4th Compressed Image of Cameraman

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a) b)

Fig 9. A) Original Lena B) 1/4th Compressed Image of Lena

REFERENCES

[1] Alice Blessie, J. Nalini and S. C. Ramesh "Image Compression Using Wavelet Transform Based on the Lifting Scheme and its Implementation", IJCSI International Journal of Computer Science Issues, Vol. 8, Issue 3, No. 1, May 2011.

[2] Sugreev Kaur and Rajesh Mehra "High Speed and Area Efficient 2D DWT Processor Based Image Compression", Signal and Image Processing: An International Journal (SIPIJ) Vol.1, No.2, December 2010 .DOI: 10.5121/sipij.2010.1203.

[3] A. Mansuri, A. Ahaitouf, and F. Abdi , "An Efficient VLSI Architecture and FPGA Implementation of High –Speed and Low Power 2-D DWT for (9,7) Wavelet Filter", IJCSNS International Journal of Computer Science and Network Security, VOL.9 No.3, March 2009 BP : 2202 FES MOROCCO.

[4] M. Jeyaprakash, "FPGA Implementation of Discrete Wavelet Transform (DWT) for JPEG 2000", International Journal of Recent Trends in Engineering, Vol 2, No. 6, November 2009.

[5] Mountassar Maamoun, Mehdi Neggazi , Abdelhamid Meraghni,and Daoud Berkani, "VLSI Design of 2-D Discrete Wavelet Transform for Area-Efficient and High speed Image Computing".

[6] Ali M. - Haj Department of Computer Engineering, "An FPGA-Based Parallel Distributed Arithmetic Implementation of the 1-D Discrete Wavelet Transform", Informatics 29 (2005) 241-247, February 2004.

[7] Jie Guo; Ke-yan Wang; Cheng- ke Wu; Yun-song Li, "Efficient FPGA implementation of modified DWT for JPEG 2000 ";9th International.

[8] Kishore Andra, Chaitali Chakrabarti", A VLSI Architecture for Lifting-Based Forward and Inverse Wavelet Transform" IEEE TRANSACTIONS ON SIGNAL PROCESSING, VOL. 50, NO. 4, APRIL 2002.

[9] Kishore Andra, Chaitali Chakrabarti, Member, IEEE, and Tinku Acharya, Senior Member, IEEE, " A VLSI Architecture for Lifting-Based Forward and Inverse Wavelet Transform", IEEE TRANSACTIONS ON SIGNAL PROCESSING, VOL. 50, NO. 4, APRIL 2002.