Design of an Efficient Optical Receiver Using Cascoded Transimpedance Amplifier

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Abstract—In this paper, optical receiver using cascoded transimpedance amplifier is proposed, which can be used for power reduction method. The presented optical receiver design achieves high power consumption, increased delay. In the optical receiver design increased delay due to the differential output driver, high power consumption due to diode connected CMOS transistors. Cascoded Transimpedance amplifier is used to design proposed optical receiver and to overcome the drawbacks of presenting optical receiver.

Index Terms—Noise cancelling Transimpedance amplifier (NC-TIA), Complementary metal oxide semiconductor (CMOS), optical receiver, cascode amplifier.

I. INTRODUCTION

Front-end preamplifiers are a critical element in optical receivers affecting the whole system performance such as Speed, Sensitivity, and Signal-to-noise ratio. Therefore, design mandates careful optimization of a number of tradeoffs between bandwidth, gain, noise, and power consumption. An Operational amplifier plays in important role in VLSI design. Op-amp adds much voltage to the voltage of the input source as it losses across the resistor. The op-amp compensates the local losses caused by the internal resistor. Transimpedance amplifiers are commonly used in receivers for optical communications to convert the current generated by a photo detector into a voltage signal for further amplification [9].

A. CMOS technology

CMOS remains one of the more mature and the cheap processes in the world. CMOS processes have improved in speed due to scaling in the past 30 years and achieved gains- bandwidth. This trend pushed the CMOS technology closer to the performance region of GaAs devices. Modern CMOS processes provide designers with many tools including a variety of active devices such as MOS varactors and passive components including spiral inductors, transmission lines and micro strip lines that were made feasible by the utilization of multiple metal layers which made the design of RF circuits possible.

Scaling of CMOS processes also caused the power supply voltages to be lowered which decreased the power dissipation of CMOS circuits considerably. Moreover the increased densities of integration combined with the reduced costs of manufacturing have made the CMOS process very popular in the design of large scale integrated circuits [5].

CMOS processes utilize MOSFET (Metal-Oxide-Semiconductor-Field-Effect- Transistor) transistors. Unlike bipolar transistors which rely on minority carrier transmission to operate and require constant biasing of the base, MOS devices use an isolated gate to form a channel by inversion between two doped terminals (n doping for NMOS and p doping for PMOS). Charge transfer is established between these terminals when a potential is applied between them. CMOS or complementary MOS uses both NMOS and PMOS devices, the latter obtained by “negating all the doping types”. MOSFETs do not require a gate current to remain on which results in low power dissipation.

B. Current to voltage conversion

In optical communications the optical signal that arrives at the receiver has to be converted into an electrical signal for further processing [3]. This process is accomplished by photodiodes that produce a current that is proportional to the power of the incident optical signal. The current produced however is usually very small and it has to be converted into a voltage signal that is large enough. In an optical receiver, the first stage that comes after the
photodiode converts the photocurrent into a proportional voltage while also adding gain. This first stage may also need to convert the single-ended signal coming from the photodiode to a differential signal depending on the architecture of the following stages. In some TIAs used in data communication, one gain stage may not be enough and further amplification by a post amplifier may be necessary in order to get a signal that has a swing that is detectable by the processing circuitry for very low power inputs. There are three main types of amplifier topologies used in optical receivers. These are high input impedance amplifiers, low input impedance amplifiers and transimpedance amplifiers. In this paper transimpedance amplifier is used.

II. OVERVIEW OF ARCHITECTURE

A. Optical receiver block diagram

The optical receiver block diagram shown in figure 1 shows NC-TIA with the post amplifiers and 50Ω drivers, (a) with external PD, (b) with integrated PD.

![Optical receiver block diagram](image)

The integrated photodiode converts light into current which is given to NC-TIA. The noise cancelling Transimpedance amplifier converts low level photodiode currents to voltages. The output of NC-TIA is given to single ended to differential amplifier and then to an output driver to increase the gain.

B. TIA with Noise Cancelling Circuitry

The TIA according to the noise cancelling (NC-TIA) was designed in 40 nm standard CMOS process. The fig.2 shows NC-TIA is formed by a three-stage inverting amplifier (M_{n1}, M_{p1}, M_{n2}, M_{n3}, Mn4, R1) with a fixed shunt feedback resistor R_{fb}=2kΩ. The input stage exploits shunt feedback (R_{fb}) across a CMOS inverter (M_{n1}, M_{p1}) to provide high gain and to achieve a low input impedance of about 65Ω. The low input impedance compensates for the large capacitance C_{PD} of the large-area PD. The input node of the input inverter stage (M_{n1}, M_{p1}) is ac coupled to the gate of M_{n3} via C_{c}=0.18 pF. M_{n3} is biased from the voltage supply through R_{B}=77kΩ. The common-source stage M_{n2}, M_{n3} implements the adder used to subtract the two noise signals coming from the input (V_{in}) and the output (V_{out}) nodes. Transistor M_{n3} also acts as a source follower, copying the voltage at the input node of the (M_{n1}, M_{p1}) stage to the output. The output of the (M_{n2}, M_{n3}) stage delivers the sum of signal voltages and the difference of the noise voltages.

The last stage is a common-source amplifier with the N-channel MOSFET Mn4 and a load resistance R1 which is selected to have a potential of 0.55V at the output and at all TIA stages as well as to achieve enough gain for the TIA to have a low input impedance.

The M_{c1} and M_{c2} NMOSFETs are used to increase the input optical power dynamic range. The M_{c1} and M_{c2} are off at low input optical power dynamic range. The M_{c1} and M_{c2} are off at low input optical power. When the input optical power increases, the control signal V_{c} switches on M_{c1} and M_{c2} M_{c3} then creates a secondary path for the generated photocurrent in addition to R_{fb}. When M_{c1} and M_{c2} are off they have the effect to decrease the bandwidth compared to TIA without M_{c1} and M_{c2} due to their parasitic capacitances. However, this technique succeeds to increase the maximum input optical dynamic range.
C. Post Amplifiers and Output Driver

There is a need for post amplifiers to obtain enough gain and for a 50 Ω driver to connect to the measurement equipment. The fig. 3 shows the differential output stage is better than a single-ended one with respect to common mode rejection and power supply noise.

III. PROPOSED METHOD

A. Cascode Amplifiers

The basic cascode amplifier consists of an input common-emitter (CE) configuration driving an output common-base (CB). The cascode amplifier also provides voltage translation of the output to a higher static (dc) voltage than the output. The output static (dc, quiescent) voltage of the complementary cascode can be same as the input because the CB BJT inverts the current polarity from the CE. This requires the addition of a bias current-source between the transistors and the current-source node floats at a junction voltage higher than \( V_B \). Consequently, \( v_{out} \) can have the same static voltage as \( v_{in} \) without offset, and the voltage supply used to implement the current source is essentially independent of the rest of the circuit. The cascode configuration also has a common source transistor at the input. The common source transistor is cascaded with a common gate transistor and a resistive load. The cascode and common source amplifiers have same gain, but the cascode will have a lower input capacitance. The cascoded transimpedance amplifier structure shown in fig.4 which has cascoded current source, photodiode at the input.
A common gate structure is normally used because it has low input impedance. By presenting the photodiode with low input impedance, the amplifier is able to isolate the photodiode capacitance from determining the bandwidth of the system. The ability of the common gate structure to isolate the large photodiode capacitance is limited by the \( g_m \) of the input transistor. In order to lower the input impedance, the size of the transistor can be increased, which raises the bias current and adds to the parasitic input capacitance.

**Fig. 4. Cascode Transimpedance amplifier**

**B. Proposed Optical Receiver Block Diagram**

The cascode amplifiers have advantages of increasing speed, and for high-voltage amplifier applications. The important performance specifications for the amplifier are a high gain, large bandwidth, low noise, and low input capacitance. In the proposed optical receiver block diagram the noise cancelling Transimpedance amplifier is replaced by cascaded Transimpedance amplifier and the following stages are same as the present optical receiver block diagram. The proposed optical receiver block diagram as shown in fig. 5. Which has cascoded TIA followed by amplifier stages to increase gain?

**Fig. 5. Proposed optical receiver block diagram**

The integrated photodiode converts light into current which is given to Cascoded TIA. The Cascoded Transimpedance amplifier converts low level photodiode currents to voltages. The output of Cascoded TIA is given to single ended to differential amplifier and then to an output driver to increase the gain. Need for post amplifiers to obtain enough gain and for a driver to connect to the measurement equipment.
IV. SIMULATION RESULTS

A. Result of Proposed Optical Receiver

The optical receiver can be designed and simulated using Tanner. First the Cascaded TIA can be designed and combined with the post amplifiers and output driver. The full schematic diagram is then simulated and power results also measured. The figure 6 shows the result of Optical receiver.

![Simulation result of Optical receiver](image)

B. Comparison of Results

By using the maximum powers obtained from the output, and time needed, the power delay product and energy delay product, Static current can be calculated. The Comparison table shows that the reduction of the MOSFET’s count, Area, Static current, PDP, EDP.

### TABLE 1

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>MOSFET'S COUNT</th>
<th>AREA (µm)</th>
<th>STATIC CURRENT (mA)</th>
<th>PDP(POWER DELAY PRODUCT) (µs)</th>
<th>EDP(ENERGY DELAY PRODUCT) (µs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPTICAL RECEIVER USING NC-TIA</td>
<td>17</td>
<td>748</td>
<td>94.227</td>
<td>1.696x10^6</td>
<td>1.696x10^13</td>
</tr>
<tr>
<td>OPTICAL RECEIVER USING CASCODED TIA</td>
<td>15</td>
<td>660</td>
<td>86.05</td>
<td>1.549x10^6</td>
<td>1.957x10^20</td>
</tr>
</tbody>
</table>

V. CONCLUSION

The proposed design and the other existing designs have been optimized and simulated extensively using a 120nm
CMOS process in a Tanner simulation environment. All the simulation specification of the parameters is used for simulation for the purpose of direct comparison between the two designs. By eliminating feedback, input matching of high frequency networks also done. The performance can be improved by reducing power consumption, the area, delay and the parasitic effects by reducing the number of transistors.

REFERENCES


