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Improved 64-Bit Binary Comparator

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Abstract*— Comparison is the most fundamental operation in most of the modern digital systems. This paper presents an improved 64-bit binary comparator which employs pipeline architecture. This brief also adds a comparison between the existing 64 bit tree based binary comparator and the modified 64 bit binary comparator presented in this paper. Comparison between the modified and existing 64 bit comparators are done using VHDL followed by Modelsim 6.3f simulations.

***Index Terms*— Comparator, Low Power, MIMO, Pre- encoder.**

I. INTRODUCTION

The comparison of two n-bit bit numbers is a critical operation for almost all digital systems. A comparator compares two n-bit values to determine which is greater, or if they are equal. In general it is used to compare two inputs. Comparators are broadly classified into Analog and Digital comparators. However in this brief what is concerned is about the digital comparator. The digital comparator is further classified into Total (Full) comparators and Equality comparators. In full comparators, given two n-bit binary numbers A and B, they are able to separately recognize the three possible conditions i.e. A > B, A < B and A = B. In equality comparators, as the name suggests, they only indicate equality when both the inputs are equal. Comparators find their applications in many Digital Signal Processors. It has been an important logic block in an ALU and have extensive applications such as decoding of x86 instructions. It also finds applications in MIMO (Multiple Input Multiple Output) decoding algorithms require extensive iterations of binary number comparison.

The 64-bit tree based comparator follows the tree structure from 2 to 64 bit. It uses a pre-encoding circuitry which is aimed to minimize the number of transistors. This design is particularly suitable for implementation with pass transistor and/or static logic to ensure low-power consumption.The modified 64-bit binary comparator has reduced area, delay and power consumption. In the modified 64-bit comparator, 64 bits are divided into eight bytes which are evaluated at the same time, and then an 8-bit comparator produces the final output signal. The rest of this brief is organized as follows: Section II reviews previous comparator works. Section III describes the 64-bit tree based comparator. Section IV introduces and explains the modified 64-bit comparator. Section V describes simulation setup and presents the delay and power simulation results. Finally, Section VI concludes with some final remarks and comments.

II. EXISTING COMPARATOR DESIGNS

In order to achieve a very high throughput, the approach proposed in [1] uses 2-phase clocking dynamic logic with all N transistors (ANT) blocks. In the ANT logic there are N blocks, the threshold voltage of transistor is variable depending on operation of entire block. Such a 64-bit transistor requires 1890 transistors and produces the correct result within 3.5 clock cycles. The main disadvantage of [1] is that it can only be implemented with heavy pipelining. Some popular microprocessors like ARM often need to execute a comparison instruction within a single clock cycle. The latches used to form the pipelines increase the circuit complexity and power consumption of the ANT comparator. A single cycle, two-phase clocking architectures are presented in [2] and [3].These comparators use a priority-encoding algorithm in [2] and a parallel MSB checking method is exploited in [3]. The latter is 22% faster than [2] but it requires 88% more transistors. In order to increase the achievable speed, a modification of MSB checking algorithm used in [3] has been proposed in [4] in which a MUX based structure has been used. This architecture is basically designed for high fan-in comparators and exhibits highest computational speed but requires 3386 transistors. The design in [4] is not suitable for static logic implementation due to tall transistor stack height. In [5] a high performance tree based comparator is proposed wherein generate (G) and propagate (P) signals can be used for binary comparisons.

III.64-BIT TREE BASED COMPARATOR

The basic comparison operation between two n-bit numbers A and B can be performed by a simple addition operation. That is, when A is greater than or equal to B, the addition operation between A and 2's complement of

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B generates a carry signal equal to 1.When A is less than B, the carry signal is 0. The low-cost addition architectures such as ripple-carry adders drastically reduce the operating speed. On the other hand, high-speed adders increase the hardware complexity. Due to this reason the design of efficient comparators doesn't employ addition logic. The circuit, for comparing two n-bit numbers, has 2n inputs and 2^{2n} entries in the truth table. The 64-bit binary comparator [5] compares two numbers each having 64 bits (A_{63} to A_0 & B_{63} to B_0). Therefore in this arrangement the truth table has 128 inputs & 2^{128} entries. The tree based comparator is designed with the logic that the generate (G) and propagate (P) signals can be employed for binary comparisons.

A. Design Principle

A two 2-bit binary number (A_1A_0 & B_1B_0) comparison can be realized with:

$$B_{big} = A_1' B_1 + (A_1 \oplus B_1)' (A_0' B_0) \quad (1)$$

$$EQ = (A_1 \oplus B_1)' (A_0 \oplus B_0)' \quad (2)$$

The three comparison signals are checked with the following conditions:
For B>A: B_{big} =1 and EQ=0; For A>B: B_{big} =0 and EQ=0; For A=B B_{big} =0 and EQ=1.
The equation (1) is similar to carry signal generation in binary addition. For instance consider the following carry generation:

$$C_{out} = AB + (A \oplus B)C_{in}$$

This implies that C_{out} can be written as:

$$C_{out} = G + P\,C_{in} \quad (3)$$

Where A and B are binary inputs, C_{in} and C_{out} are the carry inputs and carry outputs, and G and P are generate and propagate signals respectively.

Comparing (1) and (3) we have:

$G_1 = A_1' B_1$

$EQ_1 = (A_1 \oplus B_1)'$

$C_{in} = (A_0' B_0)$ for B_{big}.

The equation (1) may not be suitable for high performance operation due to complicated XNOR operation. An encoding scheme is used to solve this issue. The encoding equation is given as:

$$G_{[i]} = A_{[i]}' B_{[i]}; \; EQ_{[i]} = (A_{[i]} \oplus B_{[i]})' \quad (4)$$

Where i= 0...63. The comparison in (1) and (2) can be simplified to:

$$B_{big\,[2j+1:2j]} = G_{[2j+1]} + EQ_{[2j+1]}\, G_{[2j]} \quad (5)$$

$$EQ_{[2j+1:2j]} = EQ_{[2j+1]}\, EQ_{[2j]} \quad (6)$$

Where j= 0...31.

Therefore, Greater and EQ in a 64-bit comparator can be computed using:

$$B_{big\,[63:0]} = G_{63} + \sum_{k=0}^{63} \left(G_k \cdot \prod_{m=k+1}^{62} EQ_m \right) \quad (7)$$

$$EQ_{[63:0]} = \prod_{m=0}^{63} EQ_m \quad (8)$$

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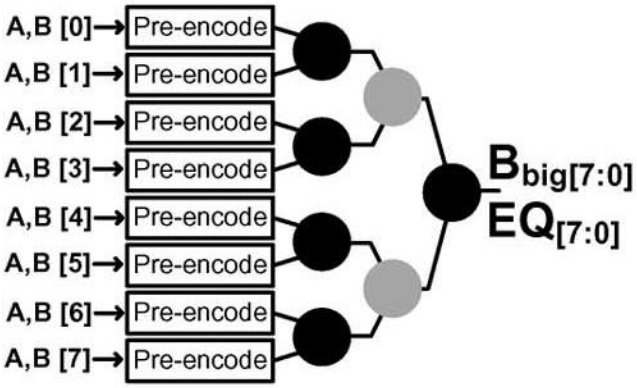

Fig.1 8-bit tree diagram of comparator

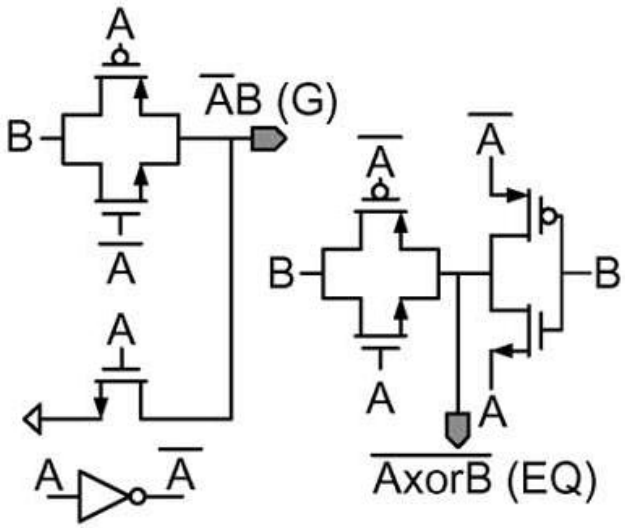

Fig.2 Pre-encode circuitry

B. Architecture

Fig. 1 demonstrates an 8-bit version of the proposed tree based comparator.Fig.2 shows the Pre-encode circuitry. 64-bit comparator is here designed in 7 stages. In the 0^{th} stage, modified pass transistor logic style circuitry is employed to produce "less than" & "equal to" outputs. The outputs of 0^{th} stage act as inputs of 1^{st} stage. In 1^{st} stage, CMOS circuitry is employed to produce inverse inputs for stage 2^{nd}. In 2^{nd} stage, CMOS circuitry is employed again to produce actual inputs for stage 3^{rd}. Now, according to tree structure given in Fig. 1, circuitry of first stage is used for third stage. Similarly, for fourth stage, circuitry of second stage is employed. For the fifth stage first stage circuitry is employed. For sixth stage the second stage circuitry employed.

IV. MODIFIED 64-BIT COMPARATOR

The proposed design strategy uses a hierarchical design of a fast 64-bit comparator is shown in Fig. 3, which is composed of eight 8-bit comparators and one final 8-bit zero/one comparator. The 64 bits are divided into eight bytes which are evaluated at the same time, and then the 8-bit comparator produces the final output signal.Fig.4, Fig.5 and Fig 6 shows the simulations for modified 64 bit comparator which depicts A<B,A=B and A>B respectively. Fig.7, Fig.8 and Fig 9 shows the simulations for modified 64 bit comparator which depicts A<B,A=B and A>B respectively

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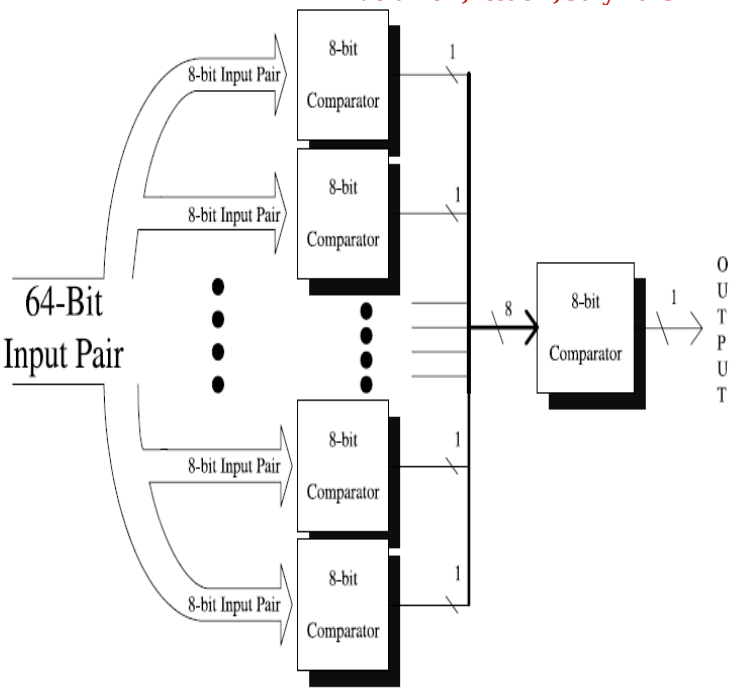

Fig.3 Modified 64-bit Comparator

V. SIMULATIONS AND COMPARISONS

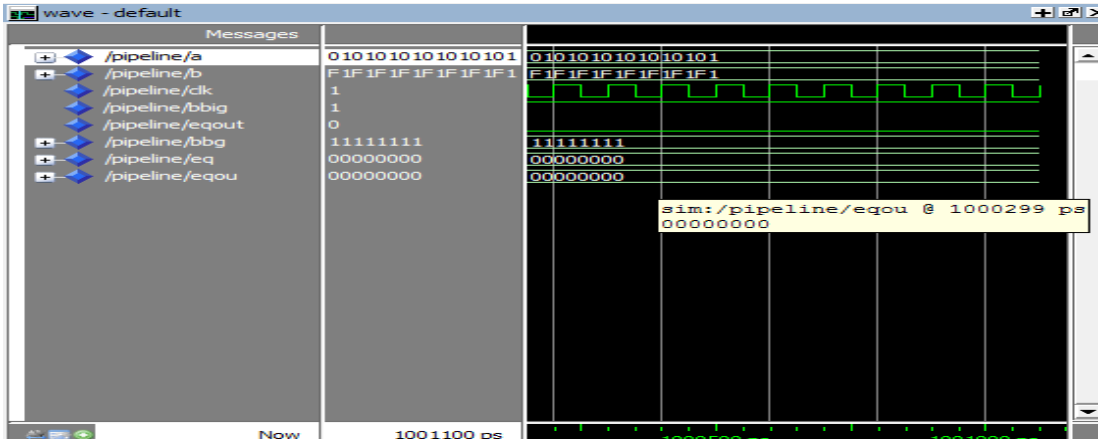

Fig.4 A<B

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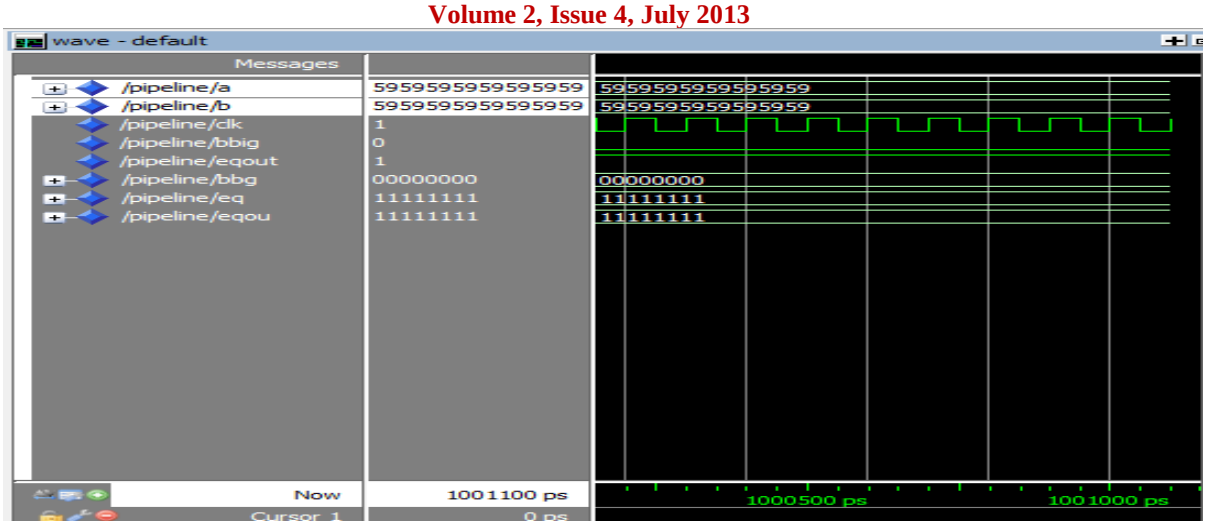

Fig.5 A=B

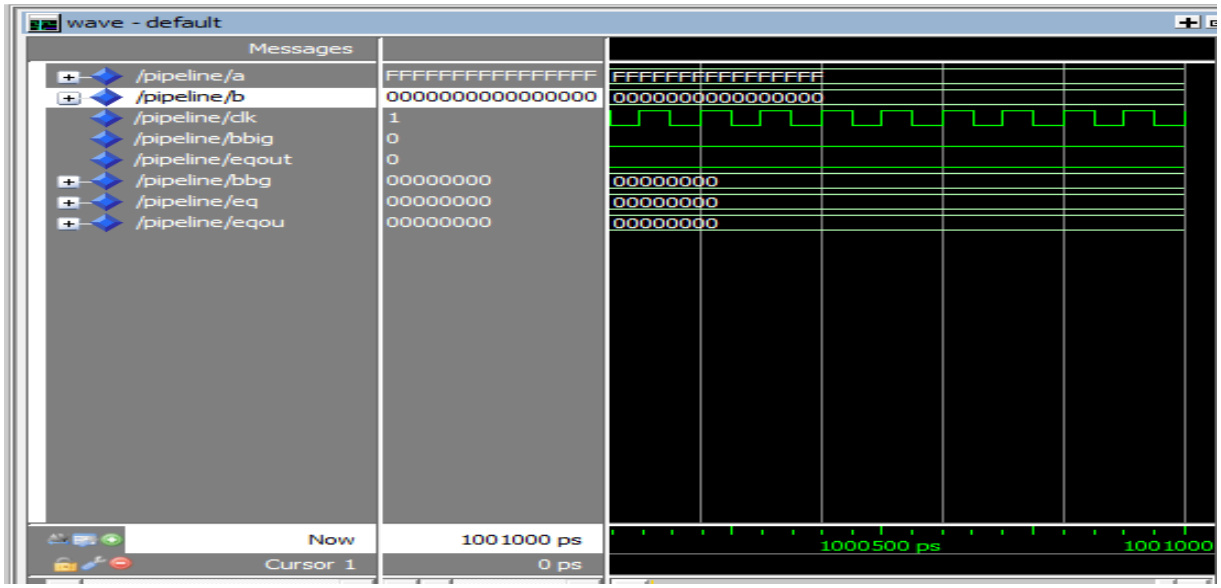

Fig.6 A >B

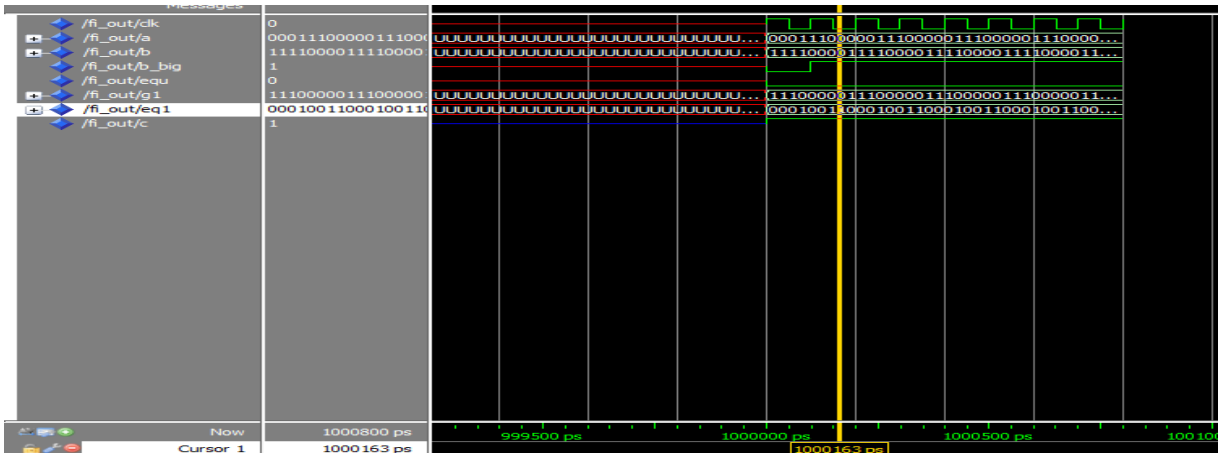

Fig.7 A <B

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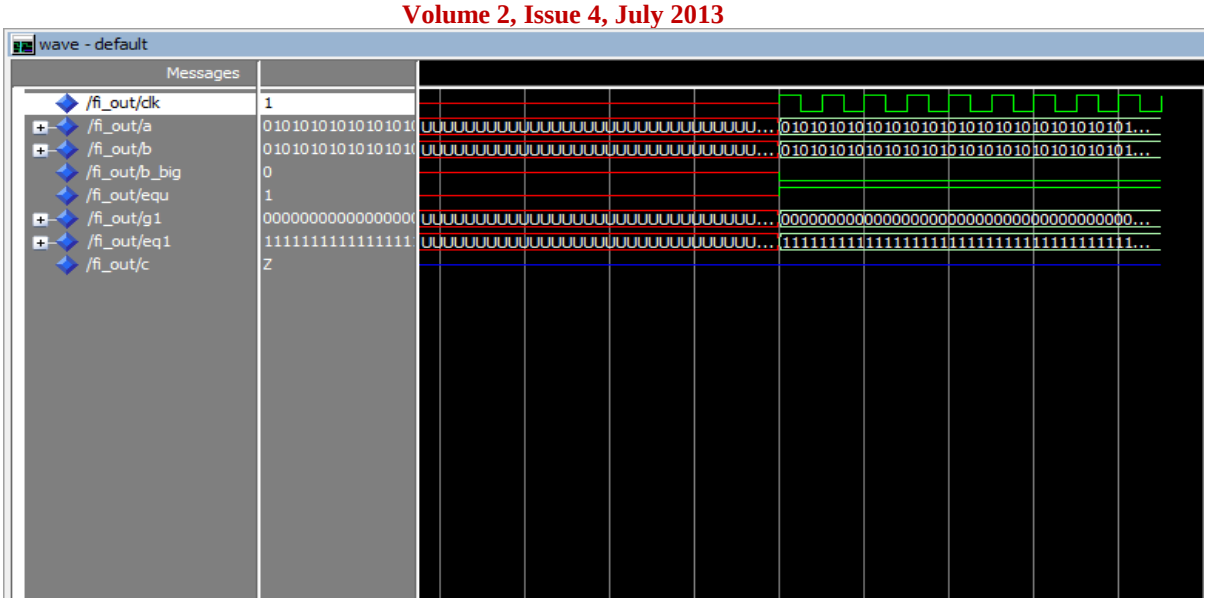

Fig.8 A =B

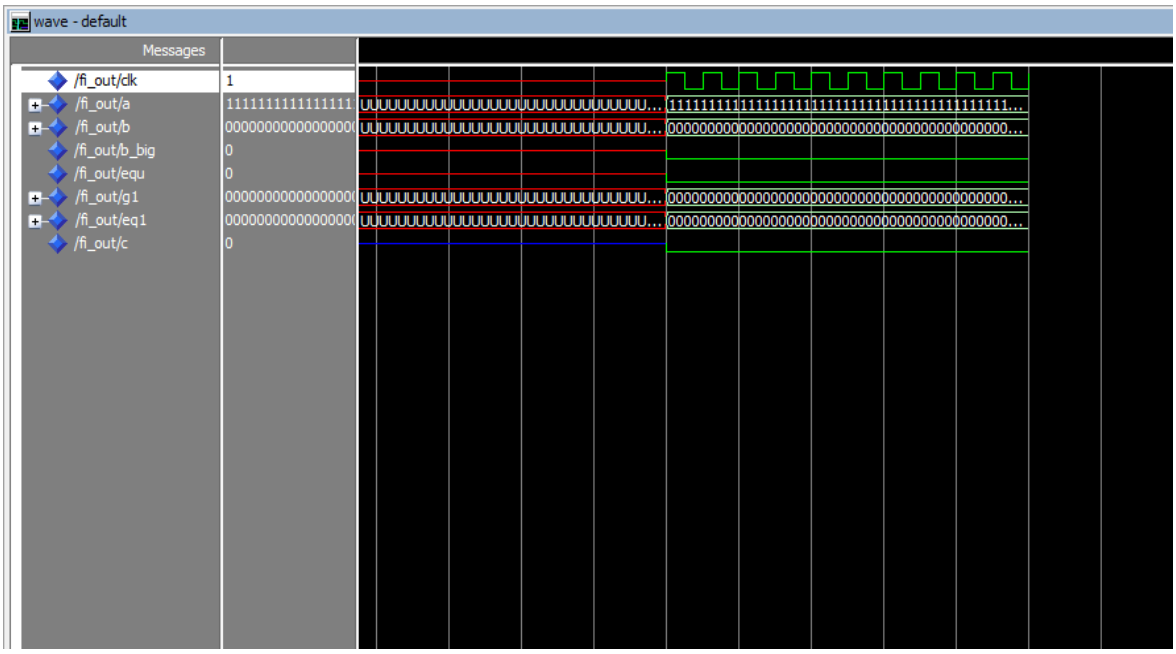

Fig.9 A >B

Table 1: Comparison

Comparator	Delay(ns)	Power(mW)	PDP(x10^-12)
Tree based comparator	7.476	1345	10055.2
Modified comparator	6.140	722	44333.08

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VI. CONCLUSION

With power and area being a limiting factor in high density and high-performance VLSI designs, a great deal of effort has been made to explore low-power and area design options without sacrificing performance. A modified 64 bit comparator is proposed in this paper. Rather than having a general scheme for comparators, different logic should be used for lower fan-in comparators and separate logic for higher fan-in comparators. The entire 64 bit is divided into groups of 8 bits each and given as input to eight comparators and a final comparator gives the output. The proposed method helps to achieve relatively large power savings over a range of supply voltage than other comparators. The comparisons of comparator design are based upon Xilinx design suite 10.1 and using Modelsim6.3 f simulations.

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