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Modified Low-Power and Area-Efficient Carry Select Adder using D-Latch

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Abstract- Carry Select Adder (CSLA) is one of the high speed adders used in many computational systems to perform fast arithmetic operations .Due to the rapidly growing mobile industry not only the faster arithmetic unit but also less area and low power arithmetic units are needed. The modified CSLA architecture has developed using Binary to Excess-1 converter (BEC). This paper proposes an efficient method which replaces the BEC using D latch. Experimental analysis shows that the proposed architecture achieves the three folded advantages in terms of area, delay and power.

Index Terms: **Low Power, CSLA, Area Efficient, BEC.**

I. INTRODUCTION

Design of area- and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position .The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. The carry-select adder (CSLA) provides a compromise between small area but longer delay ripple carry adder (RCA) and larger area with shorter delay carry look-ahead adder. CSLA uses multiple pairs of ripple carry adder (RCA) to generate partial sum and carry by considering carry input Cin=0 and Cin=1, then the final sum and carry are selected by multiplexers. The modified CSLA using BEC has reduced area and power consumption with slight increase in delay. The basic idea of the proposed architecture is that which replaces the BEC by D latch with enable signal. The proposed architecture reduces the area, delay and power. This paper is organized as follows; section III presents the detailed structure and the function of the binary to excess-1 converter logic. Section IV and section V explains the regular and modified CSLA respectively. Section VI deals with the proposed architecture. Results are analyzed in the section VII. Section VIII concludes.

II. LITERATURE REVIEW

Bedriji 1962 proposes [1] that the problem of carry propagation delay is overcome by independently generating multiple radix carries and using these carries to select between simultaneously generated sums. Ramkumar et al 2010 proposed a BEC method to reduce the maximum delay of carry propagation in final stage of carry save adder [2]. Ramkumar and Harish 2011 [7] propose BEC technique which is a simple and efficient gate level modification to significantly reduce the area and power of square root CSLA.

III.BEC

To reduce the area and power consumption of regular CSLA, RCA with Cin=1 is replaced with BEC. An n+1 bit BEC replaces the n bit RCA. The function table of a 4-b BEC is shown in Fig. 1 and Table 1 respectively. By the use of BEC logic, we can reduce the significant amount of silicon area reduction in the VLSI design. The Boolean expressions of the 3-bit BEC are given below.

S0 = ~ B0
S1 = B0 ^ B1
S2 = B2 ^ (B0 & B1)

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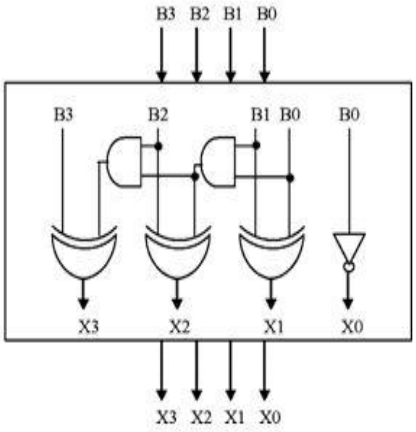

Fig. 1 4-Bit BEC

TABLE I.FUNCTION TABLE OF THE 4-BIT BEC

B[3:0]	X[3:0]
0000	0001
0001 - - -	0010 - - -
1110	1111
1111	0000

IV. REGULAR SQRT CSLA

The structure of the 16-b regular SQRT CSLA is shown in Fig. 5. It has five groups of different size RCA. The delay and area evaluation of each group are shown in Fig. 2, in which the numerals within [] specify the delay values. The carry out calculated from the last stage i.e. least significant bit stage is used to select the actual calculated values of the output carry and sum. The selection is done by using a multiplexer. Internal structure of the group 2 of regular 16-bit CSLA is shown Fig. 3. By manually counting the number of gates used for group 2 is 57 (full adder, half adder, and multiplexer). One input to the mux goes from the RCA with Cin=0 and other input from the RCA with Cin=1 The group2 has two sets of 2-b RCA. The arrival time of selection input c1 [time (t) = 7] of 6:3 mux is earlier than s3 [t = 8] and later than s2 [t = 6]. Thus, sum3 [t = 11] is summation of s3and mux [t = 3] and sum2 [t = 10] is summation of c1 and mux.

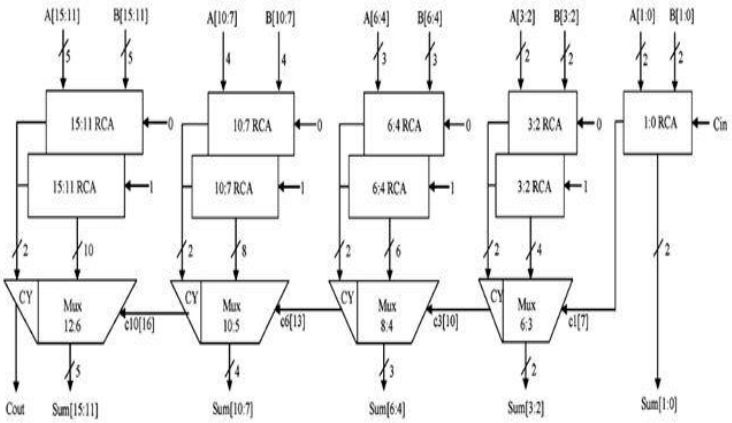

Fig.2 Regular 16 bit SQRT CSLA

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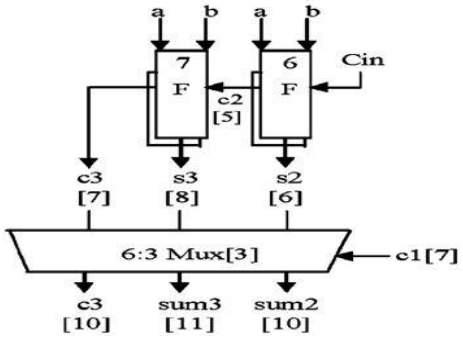

Fig.3 Group 2

V. MODIFIED CSLA USING BEC

The structure of the proposed 16-b SQRT CSLA using BEC for RCA with Cin=1 to optimize the area and power is shown in Fig. 4. We again split the structure into five groups. The delay and area estimation of each group 2 is shown in Fig. 5. One input to the mux goes from the RCA with Cin=0 and other input from the BEC. Comparing the group 2 of both regular and modified CSLA, it is clear that BEC structure reduces the area and power. But the disadvantage of BEC method is that the delay is increasing than the regular CSLA.

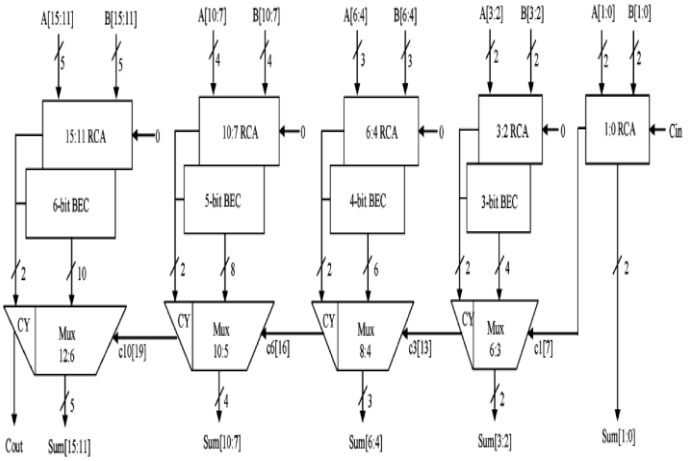

Fig. 4 CSLA using BEC

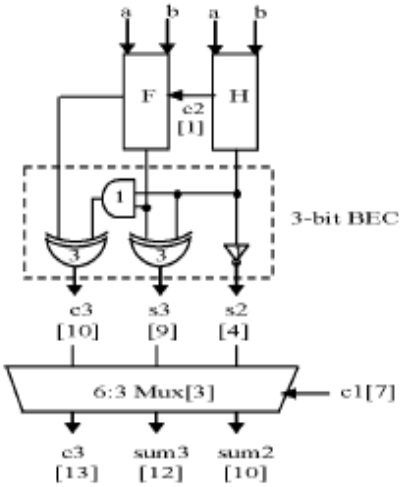

Fig. 5 Group 2

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VI. MODIFIED 16-BIT CSLA USING D-LATCH

This method replaces the BEC add one circuit by D-latch with enable signal. Latches are used to store one bit information. Their outputs are constantly affected by their inputs as long as the enable signal is asserted. In other words, when they are enabled, their content changes immediately according to their inputs. D-latch and it's waveforms are shown in Fig.6 &7.

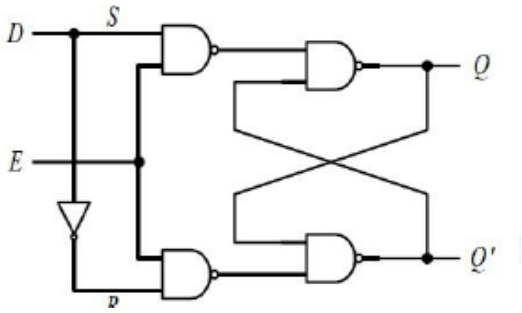

Fig.6 D-Latch

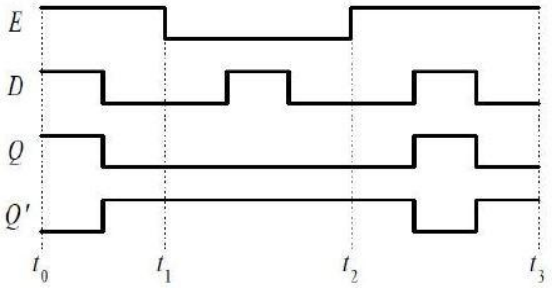

Fig.7 Input and output wave forms

The architecture of proposed 16-b CSLA is shown in Fig. 8. It has different five groups of different bit size RCA and D-Latch. Instead of using two separate adders in the regular CSLA, in this method only one adder is used to reduce the area, power consumption and delay. Each of the two additions is performed in one clock cycle. This is 16-bit adder in which least significant bit (LSB) adder is ripple carry adder, which is 2 bit wide. The upper half of the adder i.e, most significant part is 14-bit wide which works according to the clock. Whenever clock goes high addition for carry input one is performed. When clock goes low then carry input is assumed as zero and sum is stored in adder itself. From the Fig. it can understand that latch is used to store the sum and carry for Cin=1 and cin=0.Carry out from the previous stage i.e, least significant bit adder is used as control signal for multiplexer to select final output carry and sum of the 16-bit adder. If the actual carry input is one, then computed sum and carry latch is accessed and for carry input zero MSB adder is accessed. Cout is the output carry.

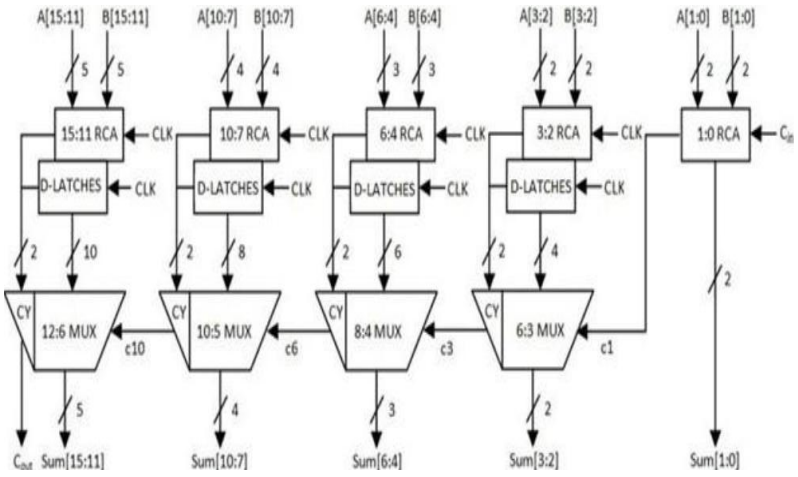

Fig.8 Modified CSLA using D-Latch

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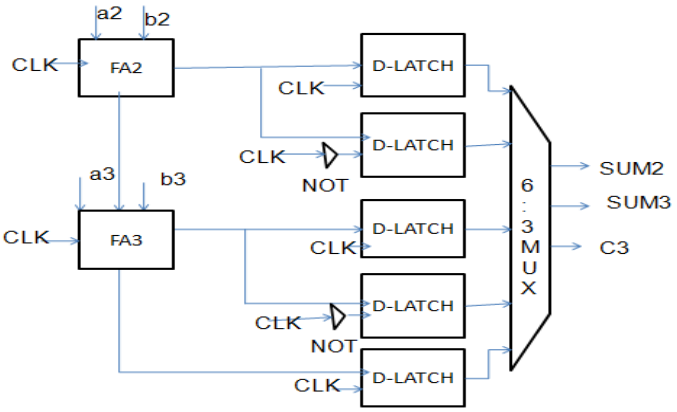

Fig. 9 Group 2

The Fig.9 shows the internal structure of group 2 of the proposed 16-bit CSLA. The group 2 performed the two bit addition which are a2 with b2 and a3 with b3. This is done by two full adder (FA) named FA2 and FA3 respectively. The third input to the full adder FA2 is the clock instead of the carry and the third input to the full adder FA3 is the carry output from FA2. The group 2 structure has five D-Latches in which four are used for store the sum2 and sum3 from FA2 and FA3 respectively and the last one is used to store carry. Multiplexer is used for selecting the actual sum and carry according to the carry is coming from the previous stage. The 6:3 multiplexer is the combination of 2:1 multiplexer. When the clock is low a2 and b2 are added with carry is equal to zero. Because of low clock, the first D-Latch is not enabled. The second D-Latch store the sum wit cin =0 by using inverted clock enable. When the clock is high, the addition is performed with carry is equal to one. The other D-Latches enabled and store the sum and carry for carry is equal to one. According to the value of c1 whether it is 0 or 1, the multiplexer selected the actual sum and carry.

VII. SIMULATION RESULTS

A. Waveform

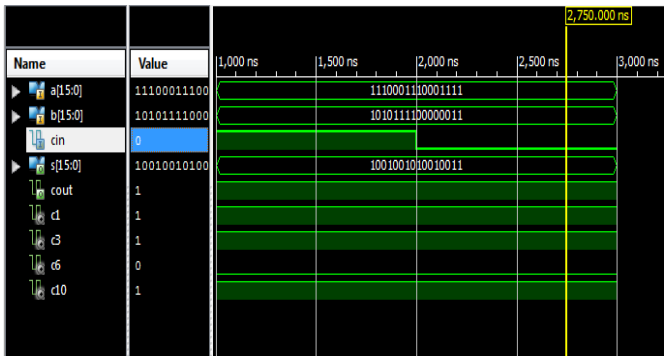

Fig.10 Regular SQRT CSLA Simulation

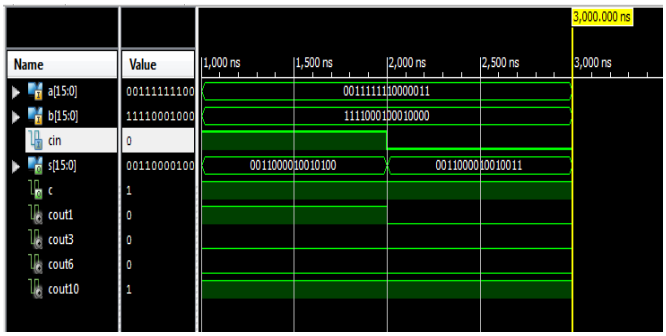

Fig.11 CSLA using BEC

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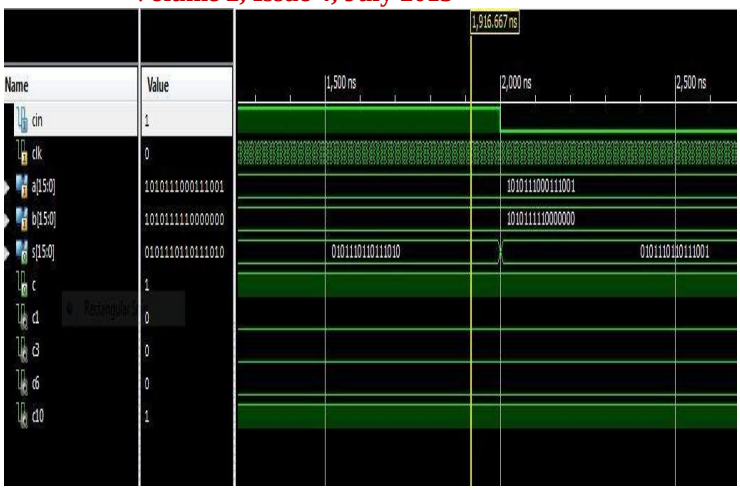

Fig. 12 Modified CSLA using D-Latch

B. Power Report

2.3. Power Supply Summary

Power Supply Summary			
	Total	Dynamic	Quiescent
Supply Power (mW)	1710.63	1654.98	55.65

Power Supply Currents

Supply Source	Supply Voltage	Total Current (mA)	Dynamic Current (mA)	Quiescent Current (mA)
Vccint	1.200	37.60	15.18	22.42
Vccaux	2.500	43.90	33.90	10.00
Vcco25	2.500	622.30	620.80	1.50

Fig .13 Power report of Regular SQRT CSLA

2.3. Power Supply Summary

Power Supply Summary			
	Total	Dynamic	Quiescent
Supply Power (mW)	874.37	827.49	46.88

Power Supply Currents

Supply Source	Supply Voltage	Total Current (mA)	Dynamic Current (mA)	Quiescent Current (mA)
Vccint	1.200	22.70	7.59	15.11
Vccaux	2.500	26.95	16.95	10.00
Vcco25	2.500	311.90	310.40	1.50

Fig.14 Power report of CSLA using BEC

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2.3. Power Supply Summary

Power Supply Summary			
	Total	Dynamic	Quiescent
Supply Power (mW)	324.21	281.48	42.73

Power Supply Currents

Supply Source	Supply Voltage	Total Current (mA)	Dynamic Current (mA)	Quiescent Current (mA)
Vccint	1.200	246.22	234.57	11.65
Vccaux	2.500	10.00	0.00	10.00
Vcco25	2.500	1.50	0.00	1.50

Fig .15 Power report of Modified CSLA using D-Latch

TABLE III
COMPARISON

Adder(16-bit)	Delay(ns)	Power(mW)	PDP(x10^-12)
Regular SQRT CSLA	20.7	1710.63	35410.04
CSLA using BEC	21.598	874.37	18884.64
Modified CSLA using D-Latch	17.84	324.21	5783.906

VIII. CONCLUSION

A simple approach is proposed in this paper to reduce the area and power of SQRT CSLA architecture. The reduced number of gates of this work offers the great advantage in the reduction of area and also the total power (Table II).The modified CSLA reduces the area and power when compared to regular CSLA with increase in delay by the use of Binary to Excess-1 converter. This paper proposes a scheme which reduces the delay, area and power than regular and modified CSLA by the use of D-latches.

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AUTHOR BIOGRAPHY

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