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Systematic VLSI Design and Implementation of Low Power High Speed Up sampler Using Multirate

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Abstract-Paper Presents Systematic VLSI design of Low Power and Area using Multirate digital signal processing system. This technique is necessary for systems with different input and output sampling rates, as the proposed multirate device is up sampler; FPGA implementation of the same is presented. The FPGA synthesis results are verified and report is presented. In order to build up sampler consisting of Shift register, D F/F and Multiplexer are downloaded on cyclone-II FPGA of ALTERA QUARTUS–II platform. The circuit obtained is verified and implemented successfully. Then it is synthesized using 45 nm library in synopsis tool with constraint of low power and area. Reduction of power consumption is important parameter for system.

Keywords: **VLSI-Very large scale integrated circuit, PCS -Personal communication services-, RTL-Register transfer logic, DSP-Digital signal processing, VHDL-Very high speed hardware description language.**

I.INTRODUCTION

Multirate digital signal processing is used in digital system where more than one sampling rate is required. It increases the efficiency of various signal processing operations. Upsampler increases the sampling rate whereas down sampler decreases the sampling rate. A discrete time system with unequal sampling rate at various node of the system called multirate signal processing .But due to the limited power-supply capability of current battery technology, PCS devices needed low-power VLSI design to minimize the total power consumption, while maintaining the system performance [1]. In general, the direct implementation of the system has a constraint that the speed of the processing elements must greater than input data rate. It cannot compensate the speed penalty under low supply voltage. On the other hand, the multirate system will require only low speed processing elements at one third of the original clock rate to maintain the same throughput [2]. Therefore, the processing elements can be operated at a lower supply voltage to reduce the power dissipation and the data throughput rate is not degraded. Basic operations of multirate processing are Upsampler, Down sampler, Decimation and Interpolation.

Up sampling: Upsampler with sampling factor L, where L is a positive integer and every L^{th} sample is taken from x[n] with all others zero which develops an output sequence $x_e[n]$ with a sampling rate that is L times greater than that of the input sequence.

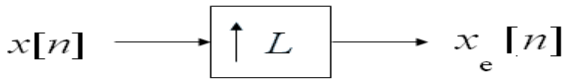

Fig. 1 Block-diagram representation

Interpolation: A process of increasing the sampling rate called interpolation. It is a method of constructing new data points within the range of a discrete set of known data points. Interpolation increase sampling rate by integer factor. Interpolation is the exact opposite of decimation. It is an information preserving operation, in that all samples of $x[n]$ are present in the expanded signal $y[n]$. The mathematical definition of L-fold interpolation is defined. Interpolation works by inserting $(L–1)$ zero-valued samples for each input sample. The sampling rate therefore increases from Fs to LFs.Expansion process is followed by a unique digital low-pass filter called an anti-imaging filter. Although the expansion process does not cause aliasing in the interpolated signal, it does however yield undesirable replicas in the signal's frequency spectrum. It depicts 3-fold interpolation of the

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signal $x[n]$ i.e. $L = 3$. The insertion of zeros effectively attenuates the signal by L, so the output of the anti-imaging filter must be multiplied by L, to maintain the same signal magnitude

II.MULTIRATE DESIGN METHODOLOGY

Multirate digital signal processing is used in sub-band coding, analog to digital/digital to analog converter, signal compression by sub sampling and voice privacy using analog phone lines. In this computational requirement are less, storage for filter coefficient is less, finite arithmetic effects are less, sensitivity to filter coefficient length is low and filter order required in multirate application is low. Since, the data rate in the multirate implementation is M-times slower than the original data rate while this feature to either the low-power implementation, or the speed-up of the DSP systems. This design methodology provides a systematic way to design low-power DSP systems at the architectural level. The multirate implementation provides a direct and efficient way to compensate the speed penalty in low-power designs at the architectural level Authors design the up sampler for low power and area .The design procedure can be extended for an arbitrary M.

III.RESULT

Implementation of the up sampler by factor M is shown as follows

Simulation of Upsampler:

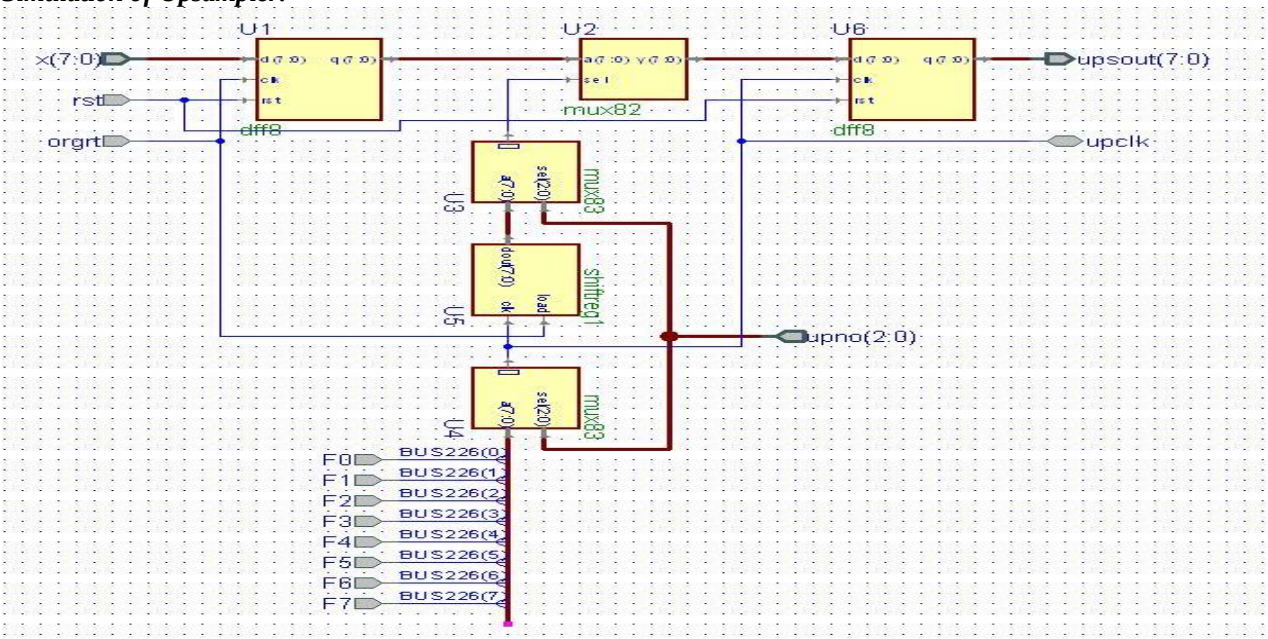

Fig. 2 Block diagram up sampler

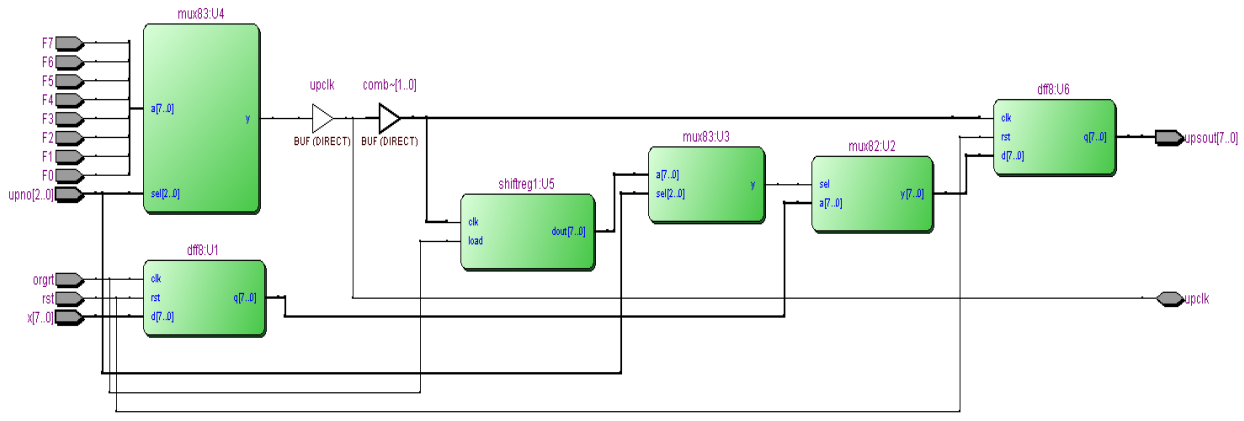

Fig. 3 RTL View of up sampler

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Simulation and Synthesis of Upsampler:

It is implemented using FPGA cyclone-II (DE-1) device and synthesized report is as follows

Flow summery

Flow Summary

Flow Status	Successful - Fri Feb 15 13:58:58 2013
Quartus II Version	10.1 Build 153 11/29/2010 SJ Web Edition
Revision Name	upsampler
Top-level Entity Name	upsampler
Family	Cyclone II
Device	EP2C20F484C7
Timing Models	Final
Total logic elements	22 / 18,752 (< 1 %)
Total combinational functions	14 / 18,752 (< 1 %)
Dedicated logic registers	17 / 18,752 (< 1 %)
Total registers	17
Total pins	30 / 315 (10 %)
Total virtual pins	0
Total memory bits	0 / 239,616 (0 %)
Embedded Multiplier 9-bit elements	0 / 52 (0 %)
Total PLLs	0 / 4 (0 %)

It is implemented using FPGA cyclone-II (DE-1) device. Synthesized report is as follows

Flow summary:

Then, it is synthesized using 45 nm library in synopsis tool with constraint of low power and area. The following report for power and area is obtained. Also, we obtained design vision schematic and encounter layout for up sampler as shown in figure 4 and figure 5.

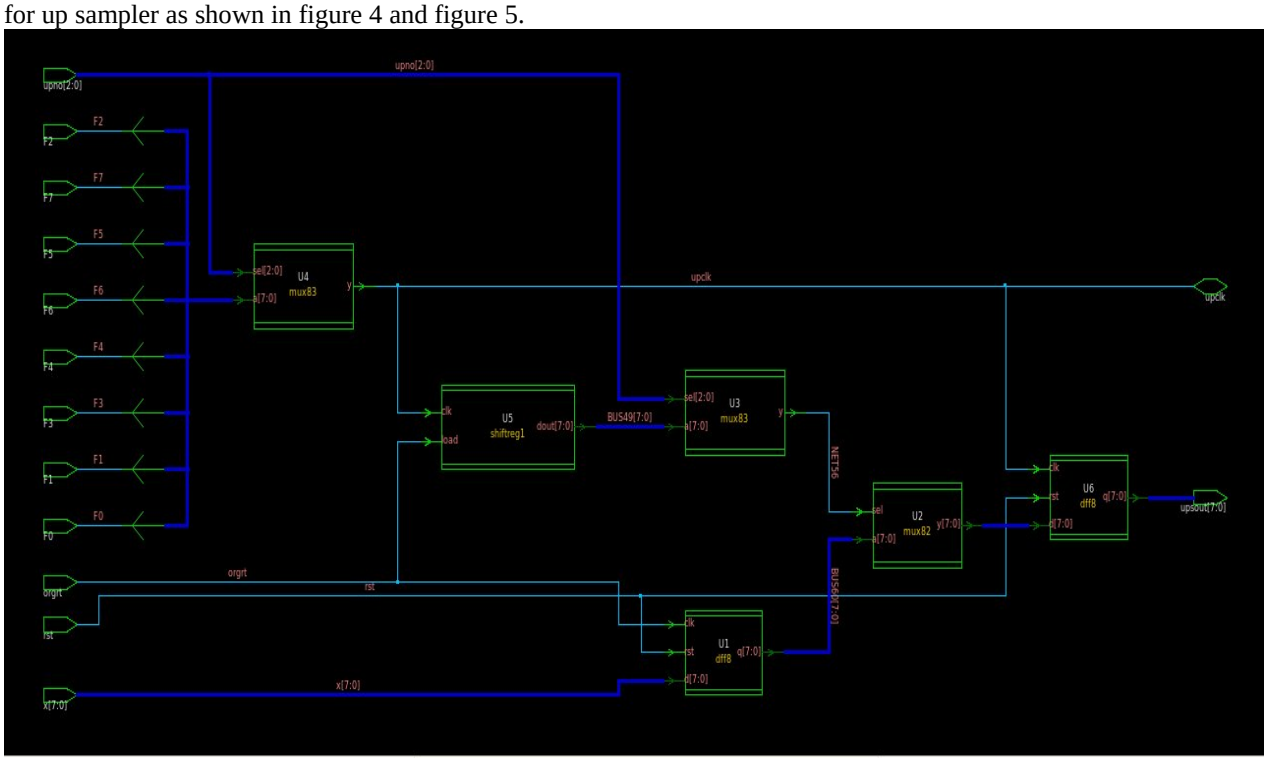

Fig.4 Design vision schematic

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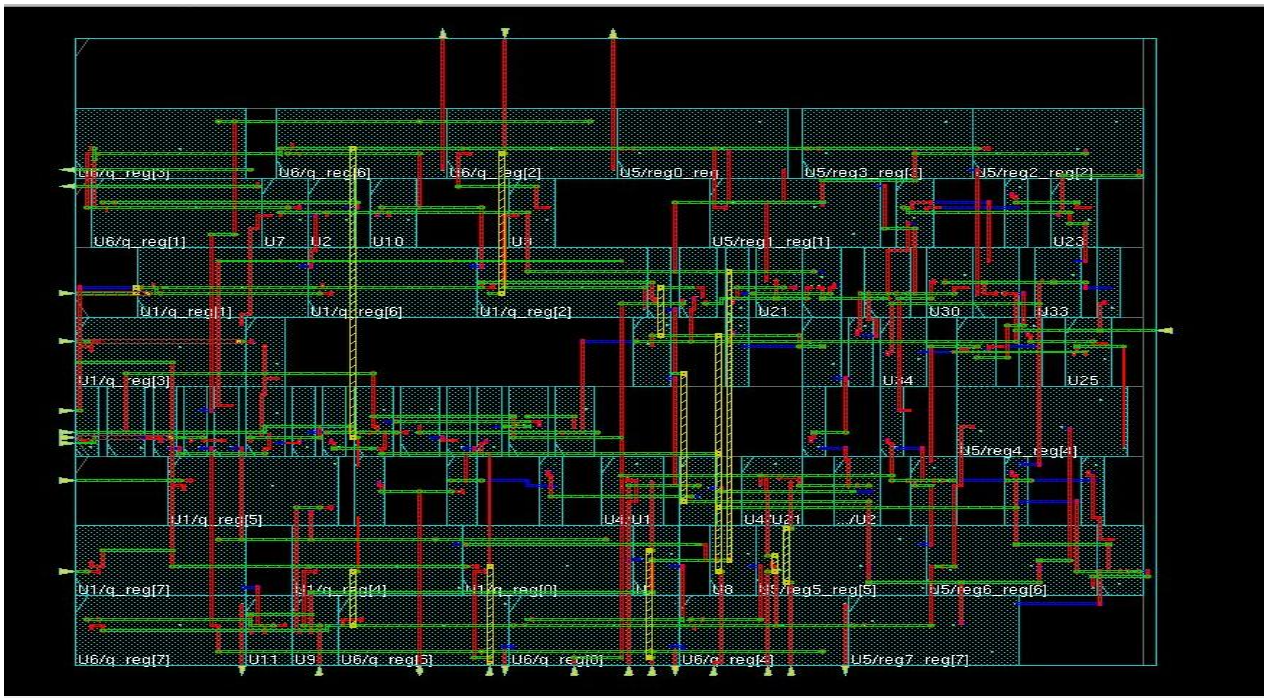

Fig. 5 Encounter Layout

Area and Power Report

Information: Updating design information... (UID-85)

****

Report: Area
Design: upsampler
Version: B-2008.09
Date : Fri Feb 15 14:21:43 2013
****

Library(s) Used:
gscl45nm (File: /home/raj/libfortech/45n/gscl45nm.db)
Number of ports: 30
Number of nets: 98
Number of cells: 55
Number of references: 10
Combinational area: 176.926096
Noncombinational area: 247.790405
Net Interconnect area: undefined (No wire load specified)
Total cell area: 424.716501
Total area: undefined

****

Report: Power
-analysis_effort low
Design: upsampler
Version: B-2008.09
Date : Fri Feb 15 14:21:59 2013
****

Library(s) Used:
gscl45nm (File: /home/raj/libfortech/45n/gscl45nm.db)
Operating Conditions: typical Library: gscl45nm
Wire Load Model Mode: top

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Global Operating Voltage = 1.1
Power-specific unit information:
Voltage Units = 1V
Capacitance Units = 1.000000pf
Time Units = 1ns
Dynamic Power Units = 1mW (derived from V, C, T units)
Leakage Power Units = 1nW
Cell Internal Power = 6.4355 uW (81%)
Net Switching Power = 1.4802 uW (19%)
Total Dynamic Power = 7.9157 uW (100%)
Cell Leakage Power = 3.5601 uW

IV.CONCLUSION

The FPGA implementation of module of upsampler with multirate signal processing approach is presented. Authors have used DE-I board with cyclone FPGA using Quartus–II platform. Authors have used synopsis tool of 45 nm library to design vision and the encounter layout. Also, design the model of upsampler with top level system design approach and low-power methodology and area for system. The results are found satisfactory. Also, the result of design of upsampler by factor found satisfactory. Physical testing verified that implementation worked correctly for all factors. The low power design using multirate approach reduces the power consumption to a great extent but it increases the hardware complexity. The proposed methodology provides a systematic way to derive low power and high speed system. For FPGA, binary to seven segment decoder is added in the design then its readability will be increased. In future, Author efforts will be directed towards transistor level implementation of multirate module to get full custom design with different circuit topology and optimization level to obtain very low power and area at high speed.

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