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FPGA Implementation of Range Resolved Algorithm

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Abstract*— This article presents development of range resolved logics to find the distance of target and its implementation on FPGA board. The measurement of the distance of target is required for various ranging applications; one of them is Laser Ceilometer. Laser Ceilometer is a system for finding the height of clouds. The Ceilometer (also known as CHI) is designed for fixed installation at airports, meteorological stations or anywhere where reliable cloud ceiling information is required. It is ideal for applications requiring highest performance and reliability such as aviation and meteorological studies and for air traffic control. In this article, first the design approach of Laser Ceilometer is presented. Then the implementation of range resolved algorithm is done on FPGA board and working principle is discussed and finally the test results are shown.

***Index Terms*— Range Resolved Logics, Ceilometer, Backscatter, FPGA.**

I. INTRODUCTION

Range Resolved Logics help in estimating the range of the targets e.g. clouds. Ceilometer is a device meant for measuring the height of clouds. Ceilometer employs a pulsed Laser Diode, where short, high repetition rate (up to 1 KHz) laser pulses [4] are sent out in vertical upward direction into the atmosphere and a detector unit is used to detect the backscattered laser return and converted optical energy into equivalent electrical energy. This received electrical signal is then passed through filtering and amplification stages. After this, the signal is digitized by using a high speed analog-to-digital converter and stored in consecutive memory locations. The reflection of light (backscatter) caused by clouds, precipitation or other obscuration is analyzed to determine the cloud base height. Then by knowing the speed of light, and time of flight, the height of the clouds can be determined.
Height of the clouds is measured by:

$$H = C * t / 2 \quad (1)$$

Here H = Cloud height
C = Speed of light
t = To and fro time

The specifications chosen for Ceilometer in this design are: Measurement Range is 5Km, Resolution is 2m and Accuracy is ±1m. Accurate measurement of cloud height in all weather conditions is must. This includes heavy precipitation and low clouds. Thus algorithms for range resolved logics need to be worked out to ensure accurate results.

II. TECHNICAL WORK PREPARATION

A. *Design Approach*

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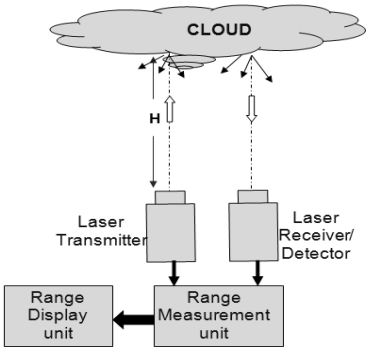

Fig.1 Block Diagram for Laser Ceilometer

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The basic components of Laser Ceilometer as shown in fig.1 are as follows:

- Laser Transmitter
- Laser Receiver/Detector
- Range Measurement Unit
- Range Display Unit

- **Laser Transmitter**

The transmitter [7] uses a 905 ±10 nm laser operated at a temperature of approximately 35°C. It employs a pulsed Laser Diode, [5] where short duration, high repetition rate laser pulses [8] are sent out in vertical upward direction into the atmosphere. A special filter is used to protect the laser diode from direct sunlight. The biggest advantage of using low power laser diode is that it provides greater eye safety.

- **Laser Receiver/Detector**

The receiver uses a 3 nm wide interference filter and several small lenses to focus the light onto a Si-APD. The reflection of light caused by clouds is analysed to determine the cloud base height by knowing the speed of light and time of flight.

- **Range Measurement Unit**

This unit is the heart of the system and basically build using Xilinx Vertex 1000E FPGA, [3] and a high speed ADC (sampling rate up to 200MHz) which measures the time interval between the transmitting signal and the receiving signal. This time interval determines the range of the target. The algorithm for measurement of range by using the transmitter and receiver signals has been developed in VHDL [1],[2] and the same has been implemented on FPGA based hardware board using JTAG.

- **Range Display Unit**

The range of target calculated in FPGA is in digital form (binary data). This binary data is then displayed on 7-segment Display by using BCD to seven segment decoder. A binary to BCD converter is also configured in the same FPGA to convert this digital data into BCD format for displaying purpose.

B. System Implementation

System implementation is done on Xilinx Vertex 1000E FPGA based Hardware board. The software tool used is Xilinx ISE 9.1i and the language code is written in VHDL.

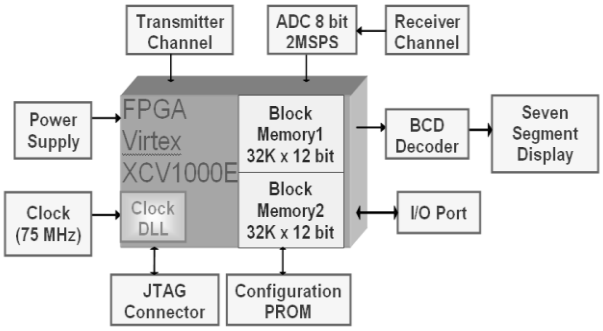

Fig. 2 Block diagram of System Implementation on FPGA Board.

Components of FPGA Board are:

- **FPGA Xilinx Vertex 1000E**

Device details

Part number : XCV1000E HQ240
Operating Frequency : 150MHz
Device type : Fast, High-Density, 1.8 V Device family, 158 I/Os

- **Analog to Digital Converter (ADC)**

Device details

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Part number : AD8200
Device type : 8 bit ADC, CMOS
Sampling frequency : 200 MSPS

- **Configuration PROM**

Device details
Part number : Xilinx XCF04S
Device type : Low power Advanced CMOS flash

- **Clock**

Device details
Part number : 75MHz oscillator
Output stability : 100ppm

- **BCD to Seven Segment Decoder**

Device details
Part number : DM74LS47N
Supply voltage : +5V

- **Joint Test Action Group (JTAG)**

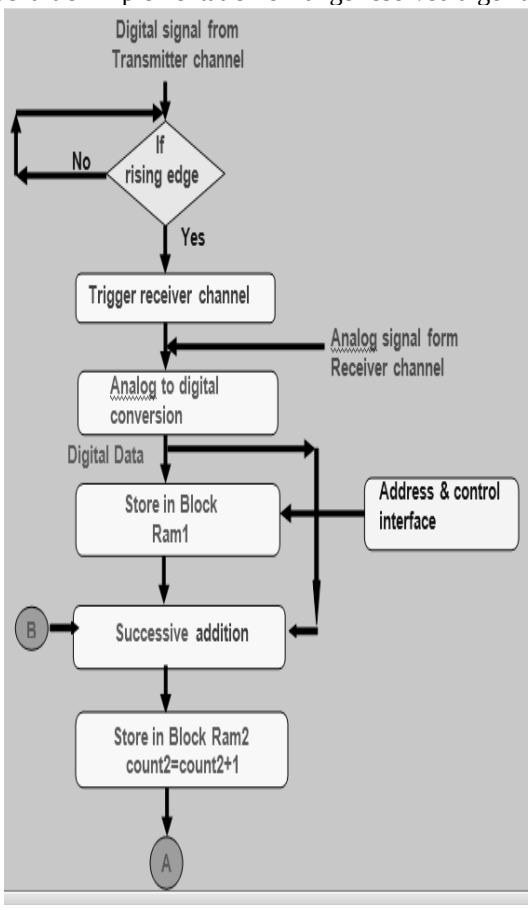
JTAG is the Development and Debug tool; need to be connected from host computers to the embedded target systems under development. This connector can also be utilized to download software code onto the FPGA board. This cable connects the parallel port of a PC to the JTAG connection of the target hardware.

- **Power Supply**

This board is powered through a 9V DC (300 mA) supply. The board has two voltage regulators that generate the 3.3V for the FPGA and 5V for the rest of the components

1) Flow chart of the Algorithm

The fig. 3 below shows the flowchart of implementation of range resolved algorithm.



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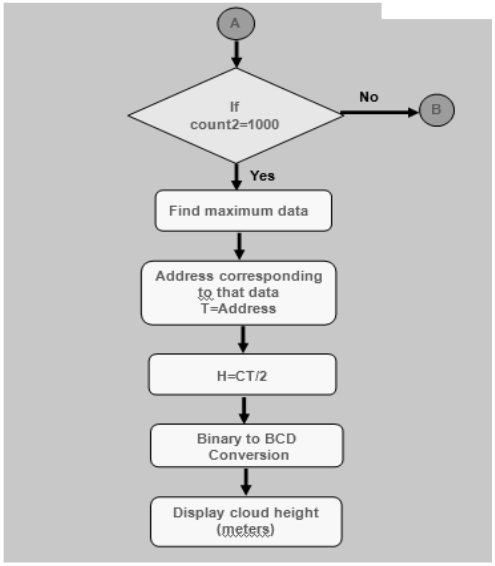

Fig.3 flowchart of implementation of range resolved algorithm

2) Working Principle

The signal processing for Laser Ceilometer is based on the principle that background noise is random in nature and it can be suppressed by repetitive measurements. The echo signal accumulates proportional to the number N of independent measurement while the noise grows only with √N. Hence by repetitive addition of echo signal, the range can be calculated.

After firing the laser, the received signal contains the information about the range of target. The received signal is amplified, sampled and digitized at regular interval, thus dividing the time axis into series of bins. The width of the bin defines the resolution of the ADC data. As the received laser pulses are very weak in strength hence first it should be amplified.

The SPU (Signal Processing Unit) consist of an 8-bit ADC to sample the input signal from the laser receiver up to 200 MSPS. The digital data is fed to the Xilinx FPGA for processing the signal in real time. Two memories (SRAMs) are used in ping-pong fashion i.e. when one is reading the data other memory is for writing the data. (Internal Block RAM can also be used instead of external memory for Fast memory reading/writing operation as required here). All addresses for the memory, data arbitration, control signal and the processing block will be implemented in the FPGA. FPGA will collect the data from the ADC in real time and store it in one of the memory. While the next set of data arrives, FPGA will pop the previous data and accumulate it with the current set of data. This accumulated value will be written into other memory. This data will be accumulated with next set of data and so on.

(Accumulated data = Accumulated data + Current data) [4]

Once all the data is accumulated in FPGA, the peak will detect using the appropriate threshold algorithm. The address of the memory location will give directly the range. Since each memory location corresponds to 2m in range (Using 75 MHz clock speed). So if memory location is 1500 at which the peak is detected, then it will give the directly the range 3000m. The range of the target will be displayed on the 7-Segment Display unit.

C. Experimental Results

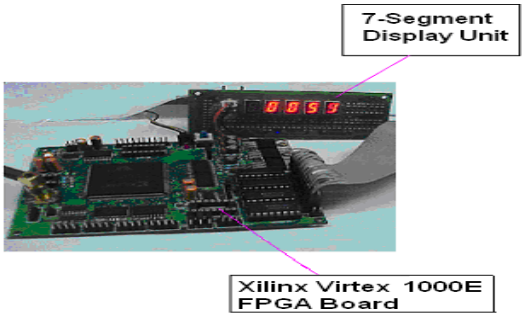

Fig. 4 Experimental set up

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Experiments have been carried out to measure the distance of the target up to 50 m with ±1m accuracy. The range of the target is then displayed on the seven segment display unit as shown in the Set up above.

III. CONCLUSION

The Ceilometer continuously monitors sky condition and reports up to four detected cloud bases and depths to an altitude of 25,000 feet above ground level. Algorithms for Laser Ceilometer have been developed and implemented to measure the distance of target on FPGA based hardware board up to a distance of 5Km. Experiments have been successfully for measuring the distance of target up to 50m with ±1m accuracy. For 1m accuracy the clock frequency required is 150 MHz. If the accuracy of 0.5m is desired then 300 MHz clock frequency is required. The results obtained from the experiments are perfectly correct. Hence, the FPGA based signal processing for Laser Ceilometer is found to be more accurate and reliable for measuring the height of clouds.

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Shikha Bathla, born in Haryana in India, on March 06, 1985. After completing, Bachelor of Technology in the field of Electronics and Communication Engineering from Kurukshetra University, Kurukshetra in 2006. She did her Masters in Technology in the field of Electronics and Communication Engineering with specialization in "VLSI Design" from Banasthali Vidyapith, Rajasthan in 2009. Presently, she is working as an Assistant Professor-1 in the Department of Electronics and Communication Engineering at Amity University, Noida. Her fields of interest lie in VLSI Design and Embedded Systems.

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