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Reduction of Multiplier in FIR Filter Using Common Sub expression Elimination Algorithm

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Abstract- In recent days filters with large lengths are started to use. So Parallel FIR filter is essential, especially when the length of the filter is large. The complexity of Finite Impulse Response (FIR) filter is dominated by the number of adders or sub tractors which are used to implement the co-efficient multipliers. A Common Sub expression Elimination (CSE) algorithm is based on the Canonical Signed Digit (CSD) representation of filter co-efficient for implementing low complexity FIR filters. Here, reduction of multiplier in linear phase FIR filters is achieved by converting the multiplier co-efficient to Minimum Signed Powers-of Two (MNSPT) or Canonical Signed Digit (CSD) representation of the multiplier. This multiplier can be implemented using a series of shifts and additions or subtractions. The CSE algorithm is used to find and eliminate more common sub expressions among filter co-efficient which results in power and area saving while implemented in FIR filters. The Common Sub expression Elimination (CSE) method to be used for the VLSI design will result in reduced multiplier in Finite Impulse Response (FIR) filter with a small number of adders and registers.

I. INTRODUCTION

Finite impulse response (FIR) filters are the most popular type of filters implemented in software. This introduction will help you understand them both on a theoretical and a practical level. Filters are signal conditioners. Each function by accepting an input signal, blocking pre-specified frequency components, and passing the original signal minus those components to the output. In a typical digital filtering application, software running on a digital signal processor (DSP) reads input samples from an A/D converter, performs the mathematical manipulations dictated by theory for the required filter type, and outputs the result via a D/A converter. Some applications need the FIR filter to operate at high frequencies such as video processing, whereas some other applications request high throughput with a low-power circuit such as multiple-input multiple-output (MIMO) systems used in cellular wireless communication. Furthermore, when narrow transition- band characteristics are required, the much higher order in the FIR filter is unavoidable. For example, a 576-tap digital filter is used in a video ghost canceller for broadcast television, which reduces the effect of multipath signal echoes. In this paper, parallel processing in the digital FIR filter will be discussed. Due to its linear increase in the hardware implementation cost brought by the increase of the block size L, the parallel processing technique loses its advantage in practical implementation.

There have been a few papers proposing ways to reduce the complexity of the parallel FIR filter in the past [1]–[7]. In [1]–[4], poly phase decomposition is mainly manipulated, where the small-sized parallel FIR filter structures are derived first and then the larger block-sized ones can be constructed by cascading or iterating small-sized parallel FIR filtering blocks. In [5]–[7], the fast linear convolution is utilized to develop the small-sized filtering structures and then a long convolution is decomposed into several short convolutions, i.e., larger block-sized filtering structures can be constructed through iterations of the small-sized filtering structures. However, in both categories of method, when it comes to symmetric convolutions, the symmetry of coefficients has not been taken into consideration for the design of structures yet, which can lead to a significant saving in hardware cost. In this paper, we provide new parallel FIR filter structures based on FFA consisting of advantageous poly phase decompositions, which can reduce amounts of multiplications in the sub filter section by exploiting the inherent nature of the symmetric coefficients, compared to the existing FFA fast parallel FIR filter structure.

II. FINITE IMPULSE RESPONSE

Filters can be classified in several different groups, depending on what criteria are used for classification. The two major types of digital filters are finite impulse response digital filters (FIR filters) and infinite impulse response digital filters (IIR).

Both types have some advantages and disadvantages that should be carefully considered when designing a filter. Besides, it is necessary to take into account all fundamental characteristics of a signal to be filtered as these are

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very important when deciding which filter to use. In most cases, it is only one characteristic that really matters and it is whether it is necessary that filter has linear phase characteristic or not. Speech signal, for example, can be processed in the systems with non-linear phase characteristic. The phase characteristic of a speech signal is not of the essence and as such can be neglected, which results in the possibility to use much wider range of systems for its processing.

The process of selecting the filter's length and coefficients is called filter design. The goal is to set those parameters such that certain desired stop band and pass band parameters will result from running the filter. Most engineers utilize a program such as MATLAB to do their filter design. But whatever tool is used, the results of the design effort should be the same: A frequency response plot, like the one shown in Figure 1, which verifies that the filter meets the desired specifications, including ripple and transition bandwidth. The longer the filter (more taps), the more finely the response can be tuned With the length, N, and coefficients, float h[N] = { ... }, decided upon, the implementation of the FIR filter is fairly straightforward. Listing 1 shows how it could be done in C. Running this code on a processor with a multiply-and-accumulate instruction (and a compiler that knows how to use it) is essential to achieving a large number of taps.

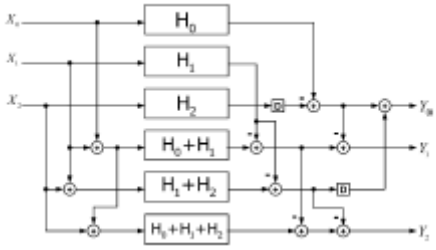

Fig 1 Parallel FIR filter architecture

III. PROPOSED RECONFIGURABLE FIR FILTER ARCHITECTURE

To utilize the symmetry of coefficients, the main idea behind the proposed structures is actually pretty intuitive, to manipulate the poly phase decomposition to earn as many sub filter blocks as possible which contain symmetric coefficients so that half the number of multiplications in the single sub filter block can be reused for the multiplications of whole taps, which is similar to the fact that a set of symmetric coefficients would only require half the filter length of multiplications in a single FIR filter. Therefore, for an N-tap 4-parallel FIR filter the total amount of saved multipliers would be the number of sub filter blocks that contain symmetric coefficients times half the number of multiplications in a single sub filter block decomposition to earn as many sub filter blocks as possible which contain symmetric coefficients so that half the number of multiplications in the single sub filter block can be reused for the multiplications of whole taps, which is similar to the fact that a set of symmetric coefficients would only require half the filter length of multiplications in a single FIR filter.

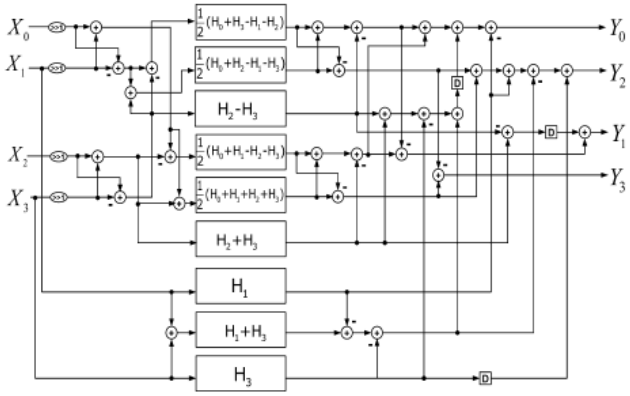

Fig. 2 Proposed parallel FIR filter architecture using four inputs

Therefore, for an N-tap 3-parallel FIR filter the total amount of saved multipliers would be the number of sub filter blocks that contain symmetric coefficients times half the number of multiplications in a single sub filter block. As can be seen from the example above, two of three sub filter blocks from the proposed two-parallel FIR filter structure,H0+H1 and H0-H1, are with symmetric coefficients now, as [6], which means the sub filter block can be realized , with only half the amount of multipliers required. Each output of multipliers responds to two taps. Note that the transposed direct-form FIR filter is employed. Compared to the existing FFA two-parallel

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FIR filter structure, the proposed FFA structure leads to one more sub filter block which contains symmetric coefficients. However, it comes with the price of the increase of amount of adders in preprocessing and post processing blocks. In this case, two additional adders are required for L==2.Add/Sub control block. This block uses the sign bit of each sub-coefficient, and control the add/sub block. To implement the multiplication by zero for each sub coefficient, the multiplexer blocks are followed by AND gates, which is controlled by Mux control block. Three full add/sub bocks are used to combine the partial products of sub coefficients

A. CSE algorithm

In this section, we will give a detailed description of an algorithm able to solve Problem B (i.e., the elimination of patterns with arbitrary shifts within the input matrix). Afterwards, we will discuss the modifications necessary for the algorithm to be able to solve Problem A as well. As indicated in the previous section, the algorithm must accomplish the following tasks.

1) Identify the presence of multiple patterns in the input matrix.
2) Select one pattern for elimination.
3) Eliminate all occurrences of the selected pattern.

This should be iteratively repeated until there are no more multiple patterns present .The input parameter represents the number of nonzero bits in the examined patterns. In the first step, an exhaustive search for all possible multiple -bit patterns is performed and complete statistics of the pattern frequencies are created.

Since many different patterns will occur more than once, some criterion must be used to select the one for elimination. We use the *steepest descent approach*, i.e., select always the pattern with the highest frequency. In the second step, all occurrences of the selected pattern are removed (i.e., the nonzero bits are replaced by zeros), and the pattern is added as a new line at the bottom of the matrix so it can be searched for the multiple patterns with smaller later. Last, since the removal of a pattern must influence the total frequency statistics of the remaining ones, the global frequency statistic holding the complete information has to be adjusted to properly reflect the changes.

After all multiple patterns with nonzero bits are processed, the whole cycle is repeated for nonzero bit patterns. A detailed discussion will be further concentrated on the following problems:

A) Pattern identification;
B) Pattern selection;
C) Frequency statistics management;
D) Adaptation of the algorithm for Problem A;
E) Viability of the algorithm for large tasks;
F) Applicability for similar CSE tasks.

IV. SIMULATION RESULTS

The design is simulated using modelsim and Xilinx. The power consumed and area utilization is calculated. The FIR Filter response using CSE algorithm shows reduced power consumption and area compared existing method. Then the performance of FFA and CSE algorithm has shown below. Using modelsim shows the output waveform of parallel FIR filter structures and symmetric coefficients with and without CSE algorithm and then the number of adders increased in FIR filter of both FFA and CSE algorithm were shown. Using Xilinx get the power consumption and area utilization of both FFA structures and CSE algorithm.

V. CONCLUSION

The CSE algorithm to reduce the number of multipliers in FIR filter structure is designed. The comparison between the FFA algorithm in FIR filter to increase the order of multipliers and CSE algorithm reduce the number of multipliers and increase the adders in parallel FIR filters are done. They can be simulated by using modelsim 6.4C and Xilinx 13.2 software and their performances were analyzed. Thus the performance of the proposed method was improved compared to the steepest descent approach. Finally, the symmetric coefficients for the parallel FIR filter using FFA is slightly increased comparing to CSE approach. The area and power consumed by CSE algorithm is less compared to the FFA algorithm using symmetric coefficients.

TABLE 1 :PERFORMANCE RESULTS FOR FFA AND CSE ALGORITHM

ALGORITHM	LENGTH 3-PARALLEL	REQUIRED MULTIPLIERS	REDUCED MULTIPLIERS	REQUIRED ADDERS		INCREASED ADDERS
				SUB	PRE/ POST	

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FFA	27-tap	46	8	48	10	5
	81-tap	136			15	
CSE	27-tap	38	26	156	10	5
	81-tap	110			15	

TABLE 2: COMPARISONS OF POWER AND AREA UTILIZATION

ALGORITHM	Power (in milli watts)	Area (in slices)
FFA	166.15	305605
CSE	129.76	280861

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