



ISSN: 2319-5967

ISO 9001:2008 Certified

International Journal of Engineering Science and Innovative Technology (IJESIT)

Volume 2, Issue 3, May 2013

Unipolar PWM Control Technique having Inverted Sine Carrier for an Asymmetric Reduced Switch Multilevel Inverter

V.Arun, B.Shanthi, S.P.Natarajan

Abstract— This paper presents a single phase asymmetrical cascaded reduced switch multilevel inverter. The proposed topology reduces the number of controlled switches used in conventional multilevel inverter and can be extended to any number of levels. Asymmetrical reduced switch multilevel inverter is triggered by the Unipolar Inverted sine PWM techniques. These Pulse Width Modulating (PWM) techniques include Phase Disposition (PD), Alternate Phase Opposition Disposition (APOD), Carrier Overlapping (CO). Performance factors like Total Harmonic Distortion (THD), VRMS (fundamental), crest factor and form factor are evaluated for various modulation indices. Simulations were performed using MATLAB-SIMULINK.

Index Terms—APOD, CO, PD, THD.

I. INTRODUCTION

Multi-level inverters are characterized by the number of different output voltage levels that can be generated by various inverter topologies. The elementary concept of a multilevel inverter achieve higher power by using a series of power semiconductor switches with several lower voltage DC sources to perform power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple DC voltage sources. The commutation of the power switches aggregates these multiple DC sources in order to achieve high voltage at the output. Aghdam et al [1] proposed multicarrier PWM methods for asymmetric multilevel inverter. Corzine et al [2] developed various control techniques for cascaded multilevel inverter. Ebrahim Babaei in [3] introduced new multilevel inverter with reduced switches. Holmes and McGrath [4] developed various Multicarrier PWM strategies for multilevel inverters. Mariethoz and Rufer [5] proposed new design and control of asymmetrical multi-level inverter. Manjrekar et al [6] developed hybrid multilevel power conversion system for high-power applications. Rodriguez et al [7] introduced various topologies and controls of multilevel inverter. Shanthi and Natarajan [8] developed unipolar PWM strategies for single phase five level cascaded inverter. Seyezhai in [9] proposed inverted sine PWM techniques for three phase asymmetric multilevel inverter. Liu et al [10] developed various algorithms for minimizing THD in multilevel inverters. The proposed topology for asymmetrical multilevel inverter has a high number of levels associated with a minimum number of switches. This paper presents a single phase reduced switch asymmetrical multilevel inverter topology for investigation using unipolar inverted sine PWM switching techniques. Simulations were performed using MATLAB-SIMULINK. Harmonics analysis and evaluation of different performance measures for various modulation indices have been carried out and presented.

II. ASYMMETRIC MULTILEVEL INVERTER

Asymmetric multi-level inverter looks like a conventional cascaded H-bridge multilevel inverter except input DC sources. The properties of asymmetric multi-level inverters are however quite different from those of symmetrical multilevel inverter. Especially the number of output-voltage levels can be dramatically increased. Instead of increasing the number of modules, one can also choose to reduce the number of cells. The advantages of asymmetric topology are:

- Reduced number of DC sources
- Low output switching frequency
- Low switching losses
- High conversion efficiency
- Flexibility to enhance output levels
- Reduction in circuit complexity and cost



ISSN: 2319-5967

ISO 9001:2008 Certified

International Journal of Engineering Science and Innovative Technology (IJESIT)

Volume 2, Issue 3, May 2013

III. PROPOSED ASYMMETRICAL MULTILEVEL INVERTER

The proposed new asymmetric cascaded multilevel inverter is shown in Figure 1. This inverter consists of a three conversion cell and a H bridge. Conversion cell consist of separate voltage sources (V_1, V_2, V_3) connected in cascade and two active switching elements that can make the output voltage in only positive polarity with several levels. H-bridge consists of four active switching elements that can make the output voltage in positive or in negative polarity depending on the switching condition. Table 1 show the switching sequence of proposed inverter.

TABLE I. SWITCHING TABLE FOR PROPOSED INVERTER

S_1	$S_{1'}$	S_2	$S_{2'}$	S_3	$S_{3'}$	A_1	B_1	A_2	B_2	Level
1	0	1	0	1	0	1	0	0	1	7
0	1	1	0	1	0	1	0	0	1	6
1	0	0	1	1	0	1	0	0	1	5
0	1	0	1	1	0	1	0	0	1	4
1	0	1	0	0	1	1	0	0	1	3
0	1	1	0	0	1	1	0	0	1	2
1	0	0	1	0	1	1	0	0	1	1
0	1	0	1	0	1	1	0	0	1	0
1	0	0	1	0	1	0	1	1	0	-1
0	1	1	0	0	1	0	1	1	0	-2
1	0	1	0	0	1	0	1	1	0	-3
0	1	0	1	1	0	0	1	1	0	-4
1	0	0	1	1	0	0	1	1	0	-5
0	1	1	0	1	0	0	1	1	0	-6
1	0	1	0	1	0	0	1	1	0	-7

IV. INVERTED SINE PULSE WIDTH MODULATION SCHEME

The scheme uses a unipolar sine modulating signal and inverted sine as carriers. In Inverted sine carrier PWM scheme, high frequency inverted sine carriers are compared with rectified sine reference. The intersection between the unipolar sine signal and the carrier signals defines the switching instant of the PWM pulse. The multiple carriers used are positioned above zero level and the number of carriers is dependent on the output voltage levels. For an m-level inverter, $(m-1)/2$ carriers with the same frequency f_c and the same amplitude A_c are disposed. The reference waveform has peak-to-peak amplitude A_m and frequency f_m . The reference is continuously compared with each of the carrier signals. If the reference is greater than a carrier signal, then the active device corresponding to that carrier is switched on; and if the reference is less than a carrier signal, then the active device corresponding to that carrier is switched off. The frequency ratio m_f are as follows: $m_f = f_c / f_m$

The advantages of ISPWM method are [9]:

- It has a better spectral quality and a higher fundamental component compared to the conventional sinusoidal PWM (SPWM) without any pulse dropping.
- The ISCPWM technique enhances the fundamental output voltage particularly at lower modulation index ranges
- There is a reduction in the total harmonic distortion (THD) and switching losses.
- To increase the fundamental amplitude in the sinusoidal pulse-width modulation the only way is by increasing the modulation index beyond 1 which is called over modulation. Over modulation causes the output voltage to contain many lower order harmonics and also makes the fundamental component vs. modulation index relation non-linear. Inverted sine pulse width modulation technique replaces over modulation.
- The appreciable improvement in the total harmonic distortion in the lower range of modulation index attracts drive applications where low speed operation is required.

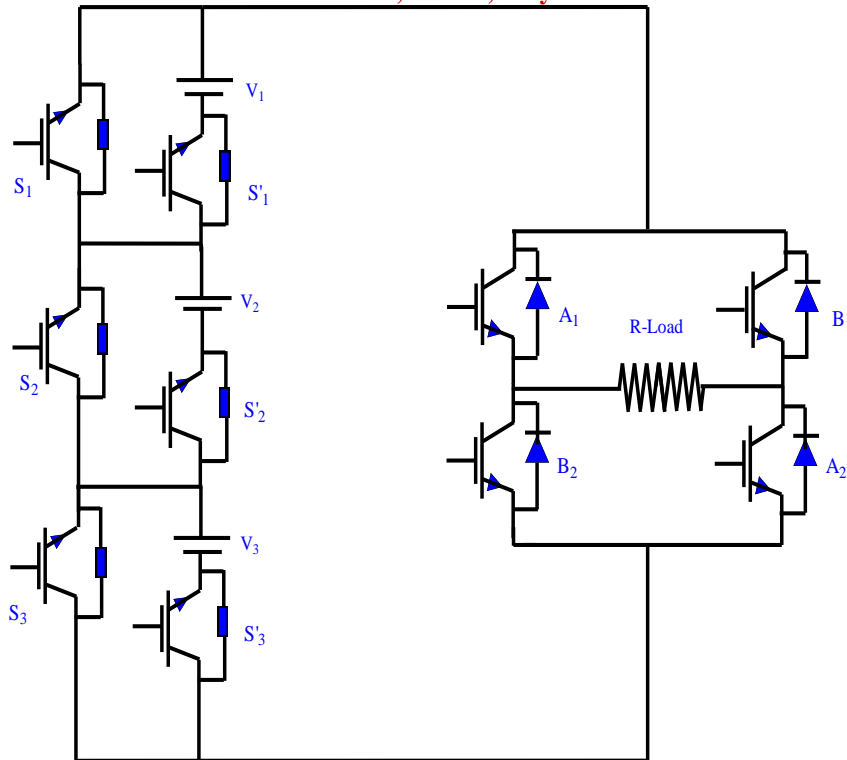


Fig 1. Proposed multilevel inverter

A. Unipolar Inverted Sine Carrier Phase Disposition PWM (UISCPDPWM)

The inverted sine carriers of same amplitude and frequency are disposed such that bands they occupy are contiguous. The carrier arrangement is shown in fig. (2). Amplitude of modulation indices $m_a = 2A_m / (m-1)A_c$

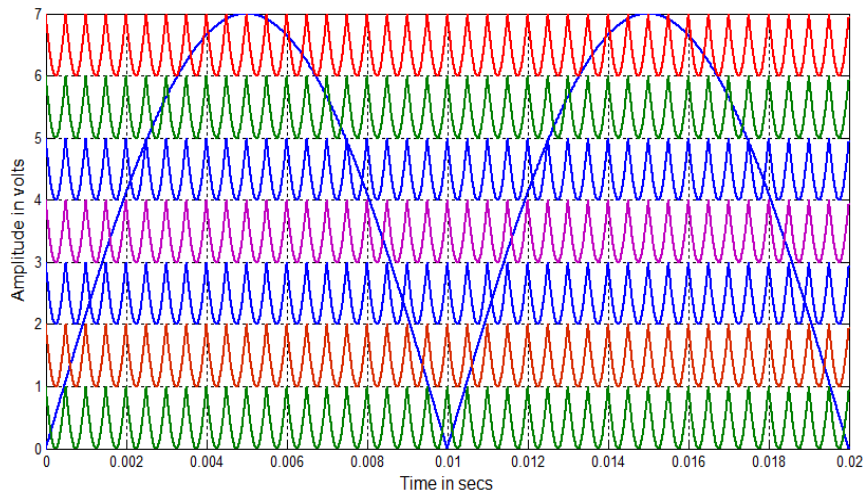


Fig.2 Carrier arrangement for UISCPDPWM Technique
($m_a=1$ and $m_f=40$)

B. Unipolar Inverted Sine Carrier Alternative Phase Opposition Dispositio PWM (UISCAPODPWM)

The inverted sine carriers of same amplitude are phase displaced from each other by 180 degrees alternately. The carrier arrangement is shown in fig. (3). Amplitude of modulation indices $m_a = 2A_m / (m-1)A_c$

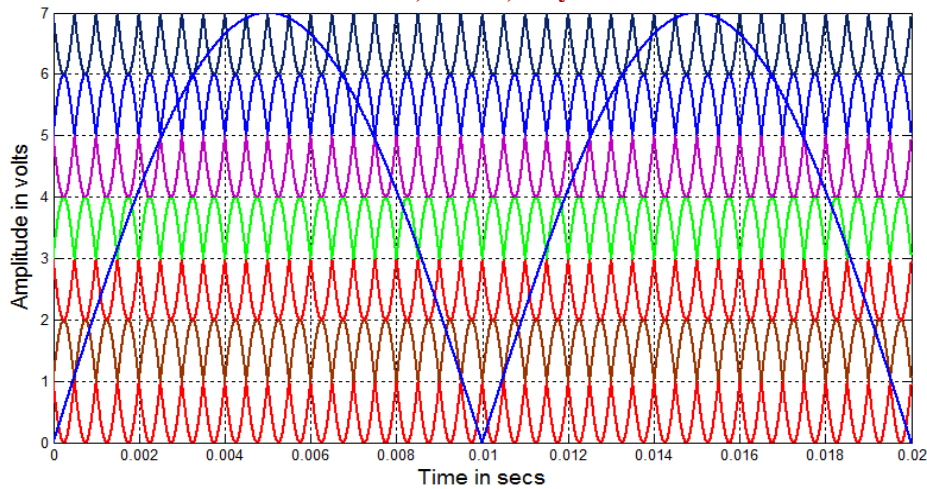


Fig.3 Carrier arrangement for UISCAPODPWM Technique
($m_a=1$ and $m_f=40$)

C. Unipolar Inverted Sine Carrier Overlapping PWM (UISCOPWM)

In carrier overlapping technique, $(m-1)/2$ carriers are disposed such that the bands they occupy overlap each other; the overlapping vertical distance between each carrier is $A_c/2$. The amplitude modulation index m_a is defined for the carrier overlapping technique are as follows: $m_a = A_m / (4 * A_c)$. Fig. (4) shows the carrier arrangement for UISCOPWM technique.

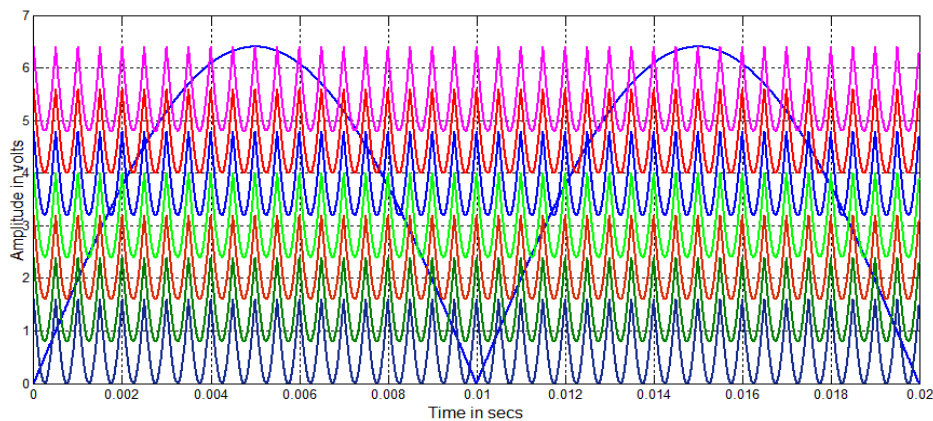


Fig.4 Carrier arrangement for UISCOPWM Technique
($m_a=1$ and $m_f=40$)

V. SIMULATION RESULTS

The single phase asymmetric reduced switch multilevel inverter is modeled in SIMULINK using power system block set. Simulations are performed for three different values of modulation indices and the corresponding %THD are measured using the FFT block and their values are shown in Table II and Figs. 5 – 10 show the simulated output voltages of asymmetric reduced switch multilevel inverter and their harmonic spectrum with above strategies but for only one sample value of $m_a = 1$. Fig. 5 shows the 15 level output voltage generated by UISCOPWM technique and its FFT plot is shown in Fig. 6. Fig. 7 shows the 15 level output voltage generated by UISCAPODPWM technique and its FFT plot is shown in Fig. 8. Fig. 9 shows the 15 level output voltage generated by UISCOPWM technique and its FFT plot is shown in Fig. 10. From Fig. 6, it is observed that the UISCOPWM technique produces significant 39th harmonic energy. From Fig. 8, it is observed that, there is no significant harmonics up to 40th order. From Fig. 10, it is observed that the UISCOPWM technique produces significant 5th, 37th and 39th harmonic energy. Tables III - V show the V_{RMS} (fundamental), Form factor (FF) and Crest Factor

(CF) for various modulation indices. It is observed (from Table II-III & Fig. 4) the harmonic output voltage is least with UISCPCPWM technique and it provides relatively higher fundamental RMS output voltage. The following parameter values are used for simulation: $V_1 = 21.5V$, $V_2 = 43V$, $V_3 = 86V$, R (load) = 100 ohms, $f_c = 2000$ Hz and $f_m = 50$ Hz.

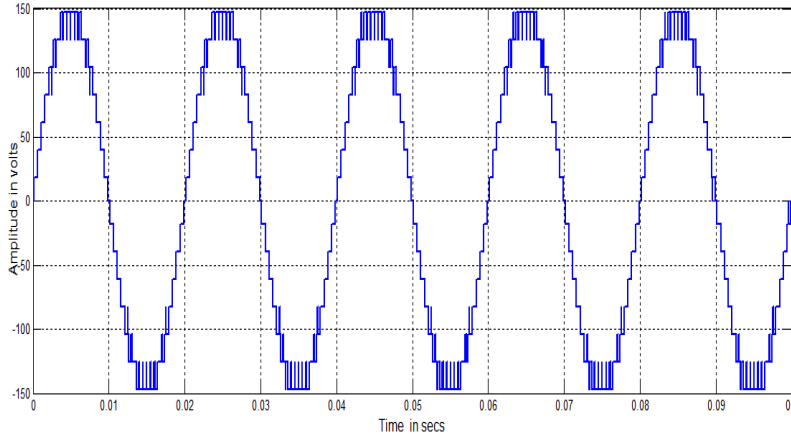


Fig 5. Simulated fifteen level output voltage generated by UISCPCPWM technique

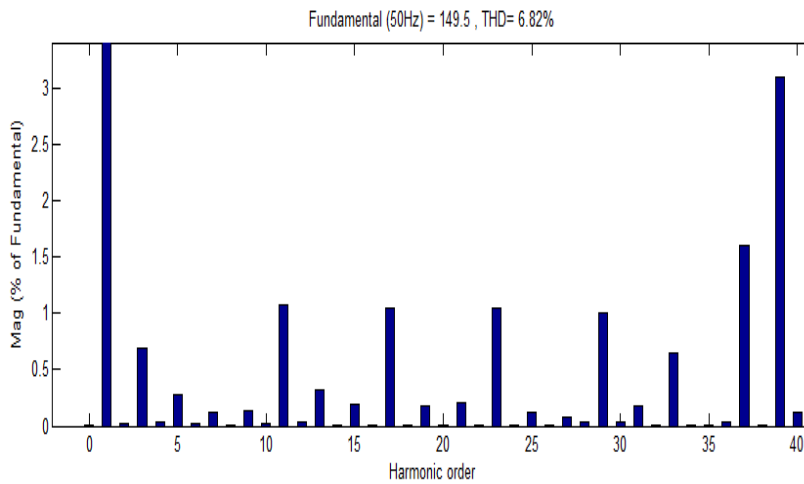


Fig 6. FFT - harmonic spectrum of output of UISCPCPWM technique

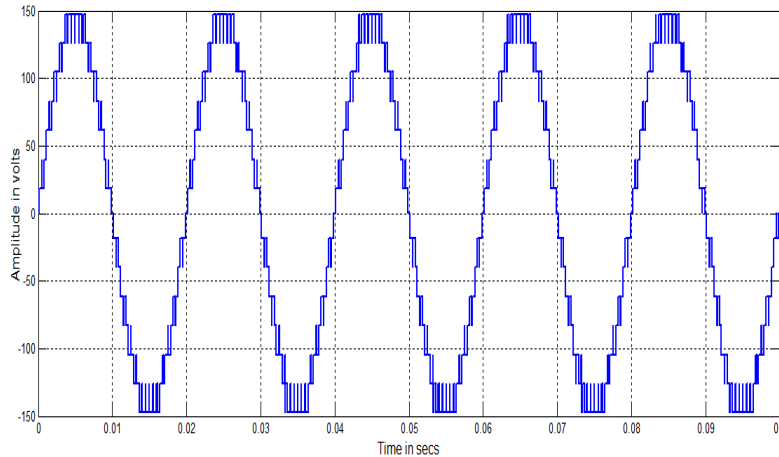


Fig 7. Simulated fifteen level output voltage generated by UISCPCPWM technique



ISSN: 2319-5967

ISO 9001:2008 Certified

International Journal of Engineering Science and Innovative Technology (IJESIT)

Volume 2, Issue 3, May 2013

Fundamental (50Hz) = 146.7, THD= 8.30%

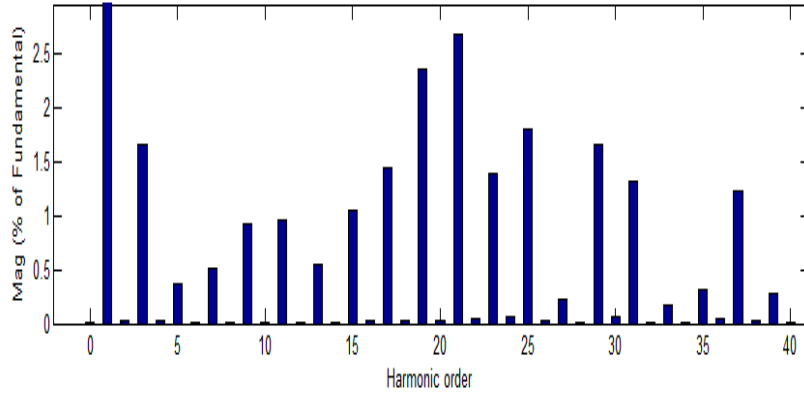


Fig 8. FFT - harmonic spectrum of output of UISCAPDPWM technique

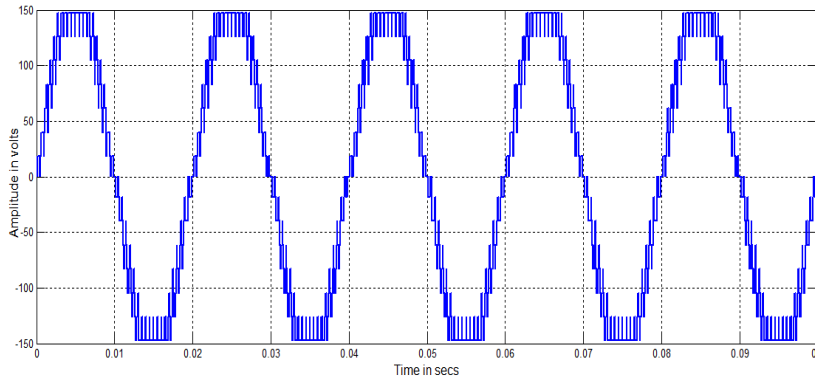


Fig 9. Simulated fifteen level output voltage generated by UISCOPWM technique

Fundamental (50Hz) = 154.7, THD= 12.14%

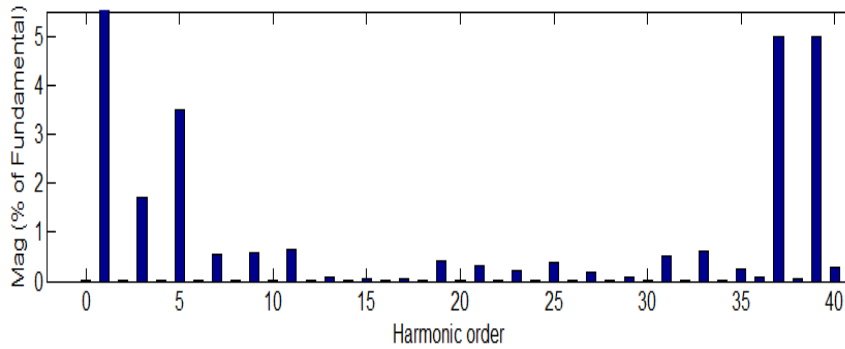


Fig 10. FFT - harmonic spectrum of output of UISCOPWM technique

TABLE II. % THD FOR DIFFERENT MODULATION INDICES

m_a	PD	APOD	CO
1	6.182	8.30	12.16
0.95	8.63	9.61	13.12
0.9	9.53	10.17	16.06



ISSN: 2319-5967

ISO 9001:2008 Certified

International Journal of Engineering Science and Innovative Technology (IJESIT)

Volume 2, Issue 3, May 2013

TABLE III. V_{RMS} (fundamental) FOR DIFFERENT MODULATION INDICES

m_a	PD	APOD	CO
1	109.7	103.7	109.4
0.95	101.9	98.95	101.5
0.9	96.39	93.99	90.52

TABLE IV. FORM FACTOR FOR DIFFERENT MODULATION INDICES

m_a	PD	APOD	CO
1	4.03E+06	1.42E+04	2.5E+04
0.95	3.7E+07	1.1E+04	7.8E+03
0.9	3.8E+04	7.15E+03	5.2E+04

TABLE V. CREST FACTOR FOR DIFFERENT MODULATION INDICES

m_a	PD	APOD	CO
1	1.3628	1.4146	1.4140
0.95	1.4141	1.4138	1.4137
0.9	1.4140	1.4139	1.4140

VI. CONCLUSION

In this paper, Unipolar Inverted sin PWM techniques for asymmetric reduced switch inverter have been presented. Proposed asymmetrical multilevel inverter gives higher output voltage level with reduced number of switches. Performance factors like %THD, V_{rms} , FF and CF have been evaluated, presented and analyzed. It is found that the UISC DPWM technique provides lower %THD and higher V_{RMS} . The proposed topology considerably reduces the number of switches for more number of levels. Switching losses, cost, and low order harmonics were considerably reduced which effectively improves the THD at the output voltage.

REFERENCES

- [1] M.G.H.Aghdam, S.H.Fathi, B.Gharehpetian, "Analysis of multicarrier PWM methods for asymmetric multilevel inverter," in Proc. 3rd IEEE Conference on Industrial Electronics and Applications, ICIEA'08, pp.2057 -2062 , 2008.
- [2] K.A.Corzine, M.W. Wielebski, F.Z Peng, and J.Wang, "Control of cascaded multilevel inverters," IEEE Trans. Power Electronics, vol.19, no.3, pp.732-738, 2004.
- [3] Ebrahim Babaei "A cascaded multilevel converter topology with reduced number of switches," IEEE Trans. Power Electronics, vol.23, no.6, 2008.
- [4] D.G. Holmes, B.P. McGrath, "Multicarrier PWM strategies for multilevel inverters," IEEE Trans. on Industrial Electronics, vol. 49, issue: 4, pp.858-867, 2002.
- [5] S.Mariethoz, and A.C. Rufer, "Design and control of asymmetrical multi-level inverters," in Proc. IEEE 28th Annual Conference, IECON 02, vol.1, pp. 840-845, 2002.



ISSN: 2319-5967

ISO 9001:2008 Certified

International Journal of Engineering Science and Innovative Technology (IJESIT)

Volume 2, Issue 3, May 2013

- [6] M.Manjrekar, P.K. Steimer, and T. Lipo, "Hybrid multilevel power Conversion System: A competitive solution for high-power applications," IEEE Trans. Ind.Applications, vol.36, no.3, pp.834-841, 2000.
- [7] J.Rodriguez, J.Lai and F.Peng, "Multilevel inverters: A survey of topologies, controls and applications," IEEE Trans. on Industrial Electronics, vol. 49, no. 4, pp. 724-738, 2002.
- [8] B.Shanthi and S.P.Natarajan, "Comparative study on various unipolar PWM strategies for single phase five level cascaded inverter," International Journal of Power Electronics (IJPELEC), Special issue on: Power Converters: Modeling, Simulation, Analysis, Topologies, Secondary issues and Applications, Inder Science Publication, Switzerland, pp.3650, 2009.
- [9] R.Seyezhai, "Inverted sine pulse width modulated three-phase Cascaded multilevel inverter," International Journal of Advances in Engineering & Technology, vol. 2, pp.602-610, 2012.
- [10] Yu Liu, Hoon Hong, and Alex Q. Huang, "Real Time algorithm for minimizing THD in multilevel inverters using unequal or varying voltage steps under stair case modulation," IEEE Trans. on Industrial Electronics, vol. 56, no.6, pp. 2249-2258, 2009.

AUTHOR BIOGRAPHY



V.Arun was born in 1986 in Salem. He has obtained B.Tech (Electrical and Electronics) and M.E (Power Systems) degrees in 2007 and 2009 respectively from SRM University, Chennai, India and Sona College of Technology, Salem, India. He has been working in the teaching field for about 4 years. His areas of interest include power electronics, digital electronics and power systems. He has 7 publications in international journals. He has presented 15 technical papers in various national / international conferences. Currently, he is working as Assistant Professor in the Department of EEE, Arunai Engineering College, Tiruvannamalai. He is a life member of Indian Society for Technical Education. Contact number- +91-9500218228. E-mail:varunpse@yahoo.com.



B.Shanthi was born in 1970 in Chidambaram. She has obtained B.E (Electronics and Instrumentation) and M.Tech (Instrument Technology) from Annamalai University and Indian Institute of Science, Bangalore in 1991 and 1998 respectively. She obtained her Ph.D in Power Electronics from Annamalai University in 2009. She is presently a Professor in Central Instrumentation Service Laboratory of Annamalai University where she has put in a total service of 20 years since 1992. Her research papers (7) have been presented in various / IEEE international / national conferences. She has 3 publications in national journal and 12 in international journals. Her areas of interest are: modeling, simulation and intelligent control for inverters. Contact number- +91-9443185211. Email: shancisl@gmail.com.



S.P.Natarajan was born in 1955 in Chidambaram. He has obtained B.E (Electrical and Electronics) and M.E (Power Systems) degrees in 1978 and 1984 respectively from Annamalai University securing distinction and then Ph.D in Power Electronics from Anna University, Chennai in 2003. He is currently Professor and Head of Instrumentation Engineering Department at Annamalai University where he has put in 31 years of service. He produced eight Ph.Ds and presently guiding eight Ph.D Scholars and so far guided eighty M.E students. His research papers 66 have been presented in various/IEEE international/national conferences in Mexico, Virginia, Hong Kong, Malaysia, India, Singapore and Korea. He has 20 publications in national journals and 43 in international journals. His research interests are in modeling and control of DC-DC converters and multiple connected power electronic converters, control of permanent magnet brushless DC motor, embedded control for multilevel inverters and matrix converters etc. He is a life member of Instrument Society of India and Indian Society for Technical Education. Contact number- +91-9443185211. Email:spn_annamalai@rediffmail.com.