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Applications of Six Sigma in Electronics Industry – A case study

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Abstract -- Six sigma is very effective tool to enhance quality performance of any process. The methodology calls for collection of historical data, analysis of data and then systematically eliminating causes of defects by using various problem solving techniques. Six sigma techniques are applicable not only for manufacturing but also for service sectors. In the case study existing process could not able to provide good first time pass of assembled Pcb during testing cycle. Systematic analysis of data along with the process parameter able to focus on the correct identification of problem and then gradually arrives at the optimum solution of the problem which resulted into considerable improvement of First time pass of assembled pcbs after testing.

Index terms: **BGA, FPGA, SMD.**

I. INTRODUCTION

In the last two and half decades, Indian organizations have faced lot of challenges due to change in international as well as domestic business scenario. Many organizations have faced hostile and challenging environment due to change in regulations, technological changes and demand of quality products from customer. All these things force organizations to rethink about strategy to align the business goal with the changing market condition. Especially Indian companies have faced a sea change in regulatory and custom regulations. As a result, many organizations have forced to adopt Quality Management Standards in response to these forces. Companies have adopted various quality management standards like Total Quality Management (TQM), Just in Time (JIT), Business process Re-Engineering (BPR), Six sigma process, Lean manufacturing, Lean six-sigma process etc. [1], [2].During the last decade, the Government of India forced many companies to compete with multinational companies both home and export market due to globalization of Industries and liberalization of import regulations. But after the liberalization process, these aspects have become imperative for very survival of many organizations. The companies in India are ever increasingly forced to achieve world class manufacturing capability in order to compete and in many cases, to survive in the market [3].

II. ELECTRONICS INDUSTRY IN INDIA

The Electronics Industry started in India around 1965 with an orientation towards space and defense technology. This was rigidly controlled and initiated by the government. This was followed by developments in consumer electronics mainly with transistor, radios, Black & White TV, calculators and other audio products. 1985 saw the advent of Computers and telephone exchanges which was succeeded by Digital electronics exchange in 1988. The period between 1984 and 1990 was the golden period of electronics, during which industry witnessed continuous and rapid growth. In recent years the electronics industry is growing at a brisk pace (30% growth per annum). India is becoming hub for manufacturing of Multinational companies like LG, Samsung, NOKIA, GE etc. The growth of Electronics Industry reported at US$ 1.75 Trillion globally is the largest and fastest growing manufacturing Industries in the world. It is expected to reach US$ 2.4 Trillion by 2020. The demand of Indian market was US$ 45 Billion in 2008-09 and is likely to reach US$ 400 Billion by 2020. The domestic production in 2008-09 was about 20 Billion but having with low values addition due to various structural changes resulting in higher costs. At the present rate of growth, the domestic production can meet to a demand of US$ 100 Billion by 2020 as against projected demand of US$ 400 Billion and balance would have to be met by imports. Demand supply gap will be nearly around US$ 300 Billion by 2020, unless the situation is improved [4]. The National Policy of Electronics, 2011 envisions creating a globally competitive Electronics System Design and Manufacturing (EDSM) industry including nano-electronics to meet the country's need and serve the international market. The major objectives are:

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Volume 2, Issue 3, May 2013

- To achieve a turnover of about 400 Billion by 2020 involving investment of about USD 100 Billion and employment to around 28 million by 2020.
- To set up over 200 Electronics Manufacturing clusters.
- To significantly upscale high- end human resources creation to 2500 PhDs annually by 2020 in the sector.

A. Challenges faced by Electronics Companies

Presently after China, India is the manufacturing hub for Electronics items assembly segment. Recently Nokia has set up plant at Chennai for assembly of mobile phone and they are in the process of expanding the plant, shifting base from China to India. Similarly there are quite a few multinational companies who are in the process of establishing Electronics assembly plants in India. The challenge for these manufacturing facilities is to manufacture item having no quality defects with least cost. In consumer electronics there is a cut throat competition with regard to price. All manufacturers try to curtail manufacturing cost. So there is a great stress in the process of manufacturing. Through put of the processes should be near to 100%. The onus lies on to process engineers/ supervisor to meet the challenges. The various types of challenges faced by the process engineers/ supervisors are:

B. Change in type of components

Around 20 years back the electronics assemblies mostly have consisted of through hole components (Leaded component) . But due to effect of automation, leaded components are changed to Surface mounted devices (SMD). It has following advantages

a. SMD shape helps for automation.
b. It occupies less space.
c. Cost effective.

Consumer electronics goods are produced in mass and due to that the production becomes cost effective [5]. The shape of components also changed to facilitate automation. More over all over the world, everybody wants electronic gadget should be smaller in shape. Component industries also rise to occasion to make component very small in size. Currently smallest size of component available in the market is 01005 size i.e 0.254 mm X 0.125 mm size, which is hardly visible in naked eye.

C. Change in process

Components are changed from through hole components to Surface mounting devices which also lead to change in assembly procedures. Through hole components used to solder by conventional soldering process using soldering iron, solder wire and flux. SMD component soldering needs machine like Screen Printer, Pick & place machine and Reflow oven. Through screen printer solder paste is applied. Pick & Place machine places components in to pcb and Reflow soldering creates bonding of component with the pcb. Earlier process was called Hand soldering process and soldering through machine is called Wave soldering process. In the advent of Surface mounted devices the soldering technique is called Reflow soldering process. The challenge for the process engineer is to arrive correct soldering profile in the reflow process such that soldering joint should be perfect without any dry solder joints or sorting or any other type of soldering defects. In SMD family, there are components like BGA (Ball Grid Arrays), LGA (Lead Less Grid Arrays) etc where the solder joints are beneath the component. Soldering these components are really challenge for process engineer. In addition to these the components are of two varieties a) Lead free component and b) Leaded component. Because of RoHS (Restriction on Hazards Substance) regulation most of the component manufacturers of European countries are switched over to lead-free substance. Based on the composition the temperature requirement varies for soldering. But still components which are used in Space, Military and Medical application are generally leaded (because of reliability issue). These components are mostly manufactured other continents than Europe. Arriving at the optimum reflow soldering profile for components having leaded and lead-free is tough ask. The eutectic point of Leaded components generally 187° centigrade and similarly eutectic point of lead-free components around 217° centigrade. When a combination of both types of components exist, the pick temperature needs to reach at least 5° to 10° more than 217° centigrade. But there are few critical components like BGA, FPGA etc; they cannot withstand temperature beyond 230° centigrade. Beyond the stipulated temperature components may get damaged. So process engineer need to manipulate temperature carefully between 220° to 228° centigrade to get optimum peak soldering profile [6].

III. INTRODUCTION TO SIX SIGMA

This concept is given by M. Harry. Six sigma is a business concept to produce high quality defect free products to the society. The processes are set in such a fashion that outcome is defect free products. There are many statistical

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International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 2, Issue 3, May 2013

methods for improving quality. Six Sigma methods get publicity when Motorola won Malcolm Baldrige Quality Award. It was further popularized by General Electric when they extensively utilized Six Sigma techniques to all most all of their processes [7]-[11].

Six Sigma is carried out in projects. The step it follows is called DMAIC (Define, Measure, Analyze, Improve and Control). First step is to define the process to be improved and after that the performance of the existing process is measured. The performance data is then analyzed. Problematic areas are identified. After analysis, improvement programme is defined and applied. Table 1 represents No. of defects with respect to Sigma [13].

Table I : Sigma specification (When the process is off –center ±1.5σ)

Specification Limit	Percentage Conformance	Nonconformance Rate (ppm)	Process Capability (Cp)
± 1σ	30.23	697700	- 0.167
± 2σ	69.13	308700	0.167
± 3σ	93.32	66810	0.500
± 4σ	99.3790	6210	0.834
± 5σ	99.97670	2330	1.167
± 6σ	99.9996600	3.4	1.500

A. *Six Sigma Case*

In order to achieve defect free throughput and to meet customer satisfaction, most of the industry is trying to adopt Six Sigma techniques in their processes [14]. Industry wants to achieve defect free through put at the minimum cost to satisfy customer expectation. Since most of the electronics industry processes are automatized, there is an effort to achieve defect free output as close to 100%. Due to this reason industries are adopting Six Sigma techniques. One case study is presented where Six Sigma techniques is successfully implemented to enhance the defect free output in a reputed Electronics Industry in India. In a Hand held radio communication set, four types of Pcbs are used. Out of these three types of Pcbs are having surface mounted devices, they are assembled through automated assembly line. The first time pass (FTP) of these pcbs are not appreciable. Because of high time consumption to repair defective pcbs, it has been decided to adopt Six Sigma techniques to improve fist time pass yield.

IV. IMPLEMENTATION AND RESULT

A. Definition of the project

- Controller Pcb of Radio set is having 107 nos of components. Out of that 104 nos are Surface Mounted devices.
- Defects of Reflow Soldered Pcbs are corrected by Hand soldering processes which consumes lot Of time as well as reduces life of solder joints.
- Being multilayer Pcbs, on many occasion the rework does not yield good result and defects like Inter layer soldering; de-lamination etc comes to light when the board are tested.
- It results in delay in production line.
- It is evident that defect free Pcbs to flow in production so that quality production moves to the Next production stage.
- Keeping all these points in mind the Project was selected.

B. *Data Analysis*

Pcb wise fault spectrum:

Data of Controller Pcb for two months was analyzed and presented in the table 2. Out of 523 Pcb offered only 393 pcb were passed in first with out any rework.

Table II: Two months data

Sl no	Qty Offered	Qty Passed	Qty Rejected
1	20	15	5
2	20	15	5
3	22	14	8
4	20	14	6
5	22	17	5
6	21	17	4

7	21	16	5
8	24	19	5
9	22	20	2
10	20	18	2
11	20	19	1
12	19	16	3
13	20	15	5
14	20	14	6
15	21	16	5
16	20	14	6
17	22	13	9
18	22	18	4
19	21	9	12
20	22	14	8
21	19	13	6
22	19	16	3
23	23	17	6
24	22	17	5
25	21	17	4
Total	523	393	130

Pareto analysis of defects:

Pareto analysis chart was made based on the type of defects observed in 130 nos of defective Pcbs.

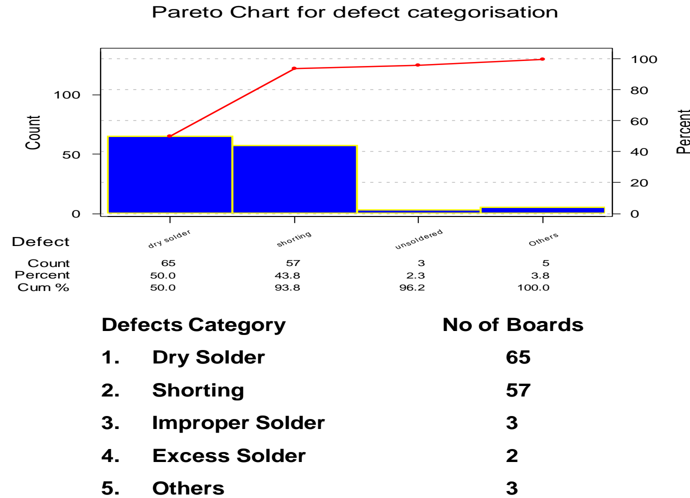

Fig. 1: Pareto Chart

Defect wise data analysis:

Each defective pcb was analyzed to find out the actual type of defects in the pcbs. The summery of all defects is shown below in Table 3.

Table III: Summary of all defects

	Defect Category	No of Defects	
Total Board Inspected : 523 Nos	1. Shorting	2480 Nos	
Passed without rework : 393 Nos	2. Dry Solder	214 Nos	
Passed after rework : 130 Nos	3. Improper solder	11 Nos	
	4. Excess Solder	10 Nos	
	5. Others	4 Nos	
		Total Defects	2719 Nos

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Volume 2, Issue 3, May 2013

Attribute Gauge R& R:

In order to establish consistency of inspection process, gauge reliability and repeatability was conducted. Two inspector were chosen randomly and for same set of Pcbs, their inspection report pattern was analyzed. Details are shown in Fig. 2. There was no significant difference in the inspection reports.

Attribute Gage R & R Effectiveness

	Attribute Legend (used in computations)			NAME:	BEL
1	pass			PRODUCT:	A2B PCB of VPS MK-III
2	fail			BUSINESS:	PROFESSIONAL ELECTRONICS
	Must match labels used below				

Known Population		Nirmal Sharma		Geeta		Y/N	Y/N
Sample #	Attribute	Try #1	Try #2	Try #1	Try #2	Agree	Agree
1	pass	pass	pass	pass	pass	Y	Y
2	fail	fail	fail	fail	fail	Y	Y
3	fail	fail	fail	fail	fail	Y	Y
4	pass	pass	pass	pass	pass	Y	Y
5	pass	pass	pass	pass	pass	Y	Y
6	fail	fail	fail	fail	fail	Y	Y
7	fail	fail	fail	fail	fail	Y	Y
8	pass	pass	pass	pass	pass	Y	Y
9	fail	fail	fail	fail	fail	Y	Y
10	fail	fail	fail	fail	fail	Y	Y
11	pass	pass	pass	pass	pass	Y	Y
12	fail	fail	fail	fail	fail	Y	Y
13	pass	pass	pass	pass	pass	Y	Y
	% APPRAISER SCORE(1) ->		100.00%		100.00%		
	% SCORE VS. ATTRIBUTE(2) ->		100.00%		100.OO%		
		SCREEN % EFFECTIVE SCORE(3) ->				100.00%	
		SCREEN % EFFECTIVE SCORE vs ATTRIBUTE (4) ->					100.00%

Fig.2: Measurement of Reliability and Repeatability

Existing process capability calculations:

Based on the available data, the process performance of existing process parameter was calculated. Zlt (Z long term) was 2.37 and Zst (Z short term) was 3.87. Detail calculation is shown in Fig.3.

CONTROLLER PCB PROCESS PERFORMANCE

1. Qty Reflow Soldered : 523
2. Defect opportunity : 573
   (Solder Joints & Comp.)
3. TOP (Total no of opportunity) : 299679
4. No of Defects : 2719
5. DPO (2719/300202) : 0.009
6. Zlt : 2.37
7. Zst (Zlt + 1.5) : 3.87

Fig.3: Calculation of process performance

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Process Flow diagram:

Process Flow diagram of Controller Pcb is shown in Fig. 4.

PROCESS MAP

LAUNCHING BY PC
COLLECTION OF MATERIAL
BAKING OF PCB IN OVEN
LOADING OF SCREEN/ SQUEZEE ON STENCIL PRINTER
FEEDER PREPRATION
SOLDER PASTE PLACEMENT ON TO SCREEN
LOADING OF FEEDER TROLLEY ON PICK & PLACE M/C
FEEDER COMPONENT VARIFICATION
NOT OK
PLACEMENT OF PCB IN MAGAZINE
SCREEN PRINTING OF PCB
PLACEMENT OF COMPONENT BY PICK & PLACE M/C
REFLOW SOLDERING
INSPECTION OF PCB
NOT OK
TOUCH UP OF PCB
OK
STORING OF PCB
MANNUAL ASSEMBLY

Fig 4. Process Map

ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 2, Issue 3, May 2013

Cause and Effect diagram:

Cause and effect diagram was prepared based on the probable cause due to which pcbs defects can occur. The diagram is shown in Fig 5.

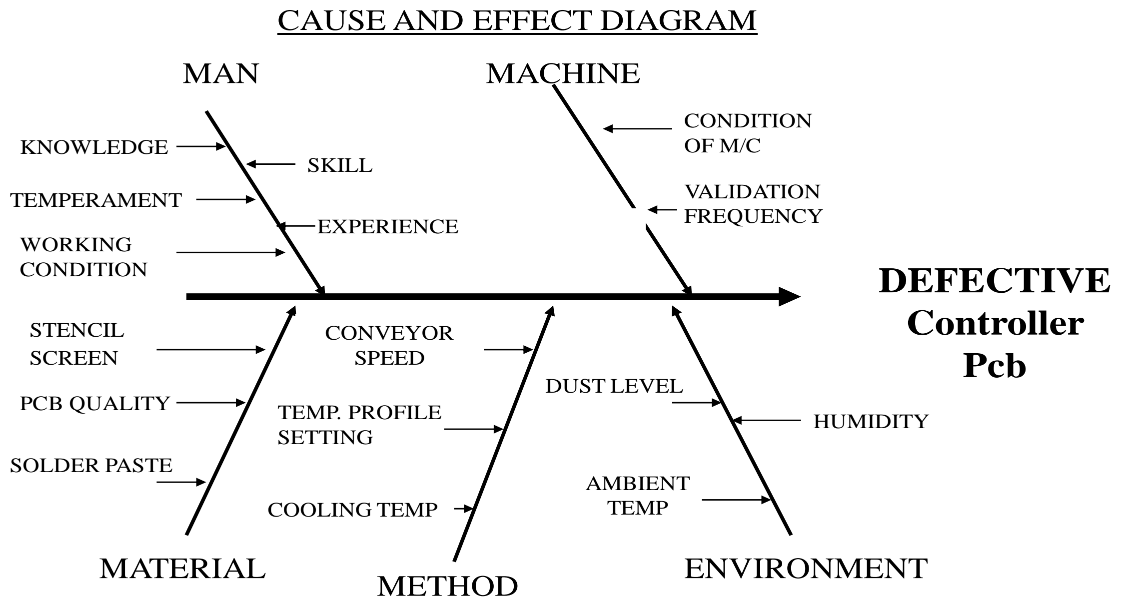

Fig 5. Cause and Effect Diagram

CNX Diagram:

A CNX diagram was made based on the cause and effect diagram. CNX diagram is shown in Fig. 6.

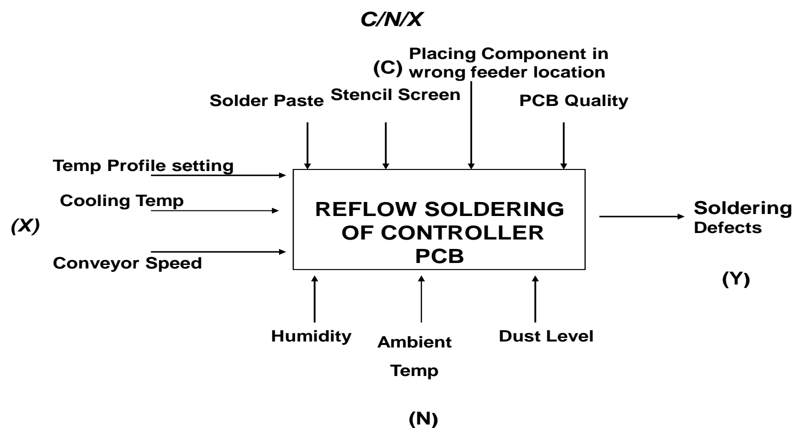

Fig. 6. CNX Diagram

Verifying Variable data in the process:

CNX diagram depicted that there were three dependent variables (X). To ascertain whether these variables are dependent or not Chi-Square Test were conducted.

ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 2, Issue 3, May 2013

In the first iteration two variables named Cooling Temperature and Conveyor speed were remain constant, only reflow oven temperature varied. Test of hypothesis reveled that since p < 0.5, hence the variable factor is significant i.e. Reflow temperature factor was significant. Details shown in Fig 7.

CHI-SQUARE Test

DIFFERENT TEMPERATURE OF HEATERS(Cooling Temp. and Conveyor speed Constant)

Sl no	qty Pass	Qty Rej	Total
1.	2	10	12
2.	9	3	12
3.	6	6	12
4.	5	7	12
5.	0	12	12
Total	22	38	60

Chi-sq = 1.309+0.758+4.809+2.784+0.582+0.337+0.082+0.047+4.400+2.547 = 17.656

DF = 4, P.Value = 0.001 (Conveyor speed = 75 cm/sec, Cooling Temp = 45 Deg C Constant).

Heater1 (° C)	Heater2 (° C)	Heater3 (° C)	Heater4 (° C)	Heater5 (° C)	Heater6 (° C)	Qty offered	Qty Rej	Qty Passed
170	180	180	180	240	260	12	2	10
170	180	190	190	245	260	12	9	3
170	180	185	185	250	260	12	6	6
170	180	195	195	250	260	12	5	7
170	180	200	200	235	260	12	0	12

CONCLUSION : P<0.05, Hence Different Temp. is 'X' Factor

Fig. 7: CHI-SQUARE Test for Temperature

In the second iteration two variables named Heating Temperature and Cooling Temperature were remain constant, only Conveyor speed was varied. Test of hypothesis reveled that since p < 0.5, hence the variable factor is significant i.e. Conveyor speed was significant. Details shown in Fig 8.

CHI-SQUARE Test

Conveyor Speed (Keeping Heating Temp. and Cooling Temperature Constant)

Sl no	Qty Pass	Qty Rej	Total
1.	6	0	6.
2.	0	6	6
3,	5	1	6
Total	11	7	18

Chi-sq = 1.485+2.333+3.667+5.782+0.485+0.762 = 14.494

DF = 2, P.Value = 0.001

Sl No	Conveyor Speed (Cm/min)	Qty Offered	Qty passed	Qty Rejected
1.	65	6	6	0
2.	70	5	1	6
3.	85	0	6	6

CONCLUSION : P<0.05, Hence Different Conveyor Speed. is 'X' Factor

Fig 8. CHI-SQUARE Test for Conveyor Speed

In the Third iteration two variables named Heating Temperature and Conveyor Speed were remain constant, only Cooling temperature was varied. Test of hypothesis reveled that p > 0.5, hence the variable factor is not significant i.e. Cooling Temperature was not significant. Details shown in Fig 9.

CHI-SQUARE Test

Different Cooling Temperature (Keeping Heating Temp. and Conveyor Speed Constant)

Sl no	Qty Pass	Qty Rej	Total

ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 2, Issue 3, May 2013

1.	6	0	6.
2.	4	2	6
3,	4	2	6
Total	14	4	18

Chi-sq = 0.381+1.333+0.095+0.333+0.095+0.333 = 2,571
DF = 2, P-Value = 0.276

DATA

	Cooling Temp.	Qty Off	Qty Passed	Qty Rej
Heater temp. 170 180 190 190 245 260	45 Deg	6	6	0
(Deg C)	50 Deg	6	4	2
Conveyor Speed – 75 Cm/Min	55 Deg	6	4	2

CONCLUSION : P > 0.05, Hence Different Cooling Temp. is not 'X' Factor

Fig 9: CHI-SQUARE Test for Cooling Temperature

New CNX Diagram:

The new CNX diagram was arrived after conducting Cho-Square test on the data. In the modified CNX diagram, there are only two variable factors (Heating Temperature and Conveyor speed). Diagram is shown in Fig 10.

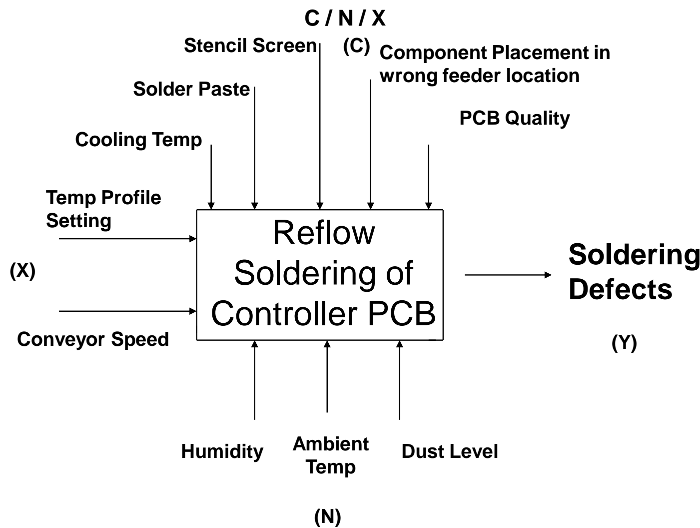

Fig 10. New CNX Diagram

Solution for Constants:

Solution for Constants are mentioned below.

Solution for Constants

1. Cooling Temperature: Cooling Temperature to be maintained at 45degree centigrade.
2. Solder Paste :
   a. Check the expiry of solder paste.
   b. Store solder paste in refrigerator when not in use.
   c. Screen printing, mounting the component and soldering of the component should be continuous process without any unusually long gap in between each operation.
3. Stencil Screen :
   a. While manufacturing Templates use Solder paste pcb negatives.
   b. Screen to be manufactured out of stainless steel sheets of thickness as per IPC standards.
   c. Fine pitch components aperture size should be as per IPC Standards.
   d. Templates to be mounted on the frame fully stretched from all sides without leaving any bends.
4. Components Placement in wrong Feeder location :
   a. Mention component part no on tape and paste near feeder location.

ISSN: 2319-5967

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International Journal of Engineering Science and Innovative Technology (IJESIT)

Volume 2, Issue 3, May 2013

b. Keep all components marked with proper part no.

5. Pcb quality :

a. Check the quality of Tin plating on the pad before use.

Design of Experiments:

Parameter for design of experiment are given below.

PARAMETER FOR DESIGN OF EXPERIMENTS

1. *Main Factors* : The reflow oven is having 6 zones, first three zones are preheating zones and last three are called peak zones. The temperature profile mostly depend upon temperature of last three zone. Hence only last three zone temperatures are taken as main factors along with the conveyor speed.

a. Temperature (° C) T1, T2, T3

b. Conveyor Speed (Cm/Min)

2. *Selection of Design* : 2*4 = 16 Iterations (Full Factorial)

3. *Range of Factors selected for design of Experiments:*

Factors		Minimum (-1)	Maximum (+1)
Temperature (° C)	T1 T2 T3	180 190 255	200 200 265
Conveyor Speed (Cm/Min)	S1	75	85

Factorial Design :

Factorial design values are shown in Fig 11.

DOE FOR CONTROLLER PCB

2^4 FRACTIONAL FACTORIAL DESIGN

T1	T2	T3	S1	R1	R2	R3	Y-AVG	S D
180	200	265	85	176	165	184	175	9.53
180	190	255	85	146	152	159	152.33	6.5
180	190	265	85	32	31	35	32.66	2.08
180	200	265	75	148	156	150	151.33	4.16
180	190	255	75	104	105	97	102	4.35
200	200	255	85	12	8	9	9.67	2.08
180	190	265	75	29	32	30	30.33	1.52
200	190	265	75	28	32	30	30	2
200	200	265	75	186	175	170	176.66	7.63
200	200	255	75	12	8	6	8.66	3.05
200	190	265	85	148	152	150	150	2
200	190	255	85	18	26	21	21.66	4.04
200	190	255	75	12	16	15	14.33	2.08
200	200	265	85	149	147	144	146.66	2.51
180	200	255	85	8	12	10	10	2
180	200	255	75	3	3	6	4	1.73

Fig 11. Factorial Design

Main Effect diagram:

Main effect diagram of variable temperature is shown in Fig 12.

ISSN: 2319-5967
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International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 2, Issue 3, May 2013

Main Effects for Y-AVG

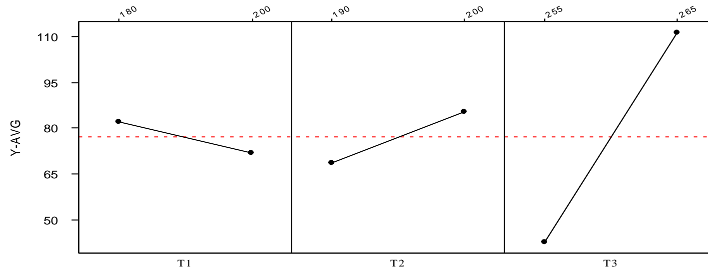

Fig. 12: Main Effect Diagram

Interaction diagrams :

Interaction diagrams among variables is shown in Fig 13.

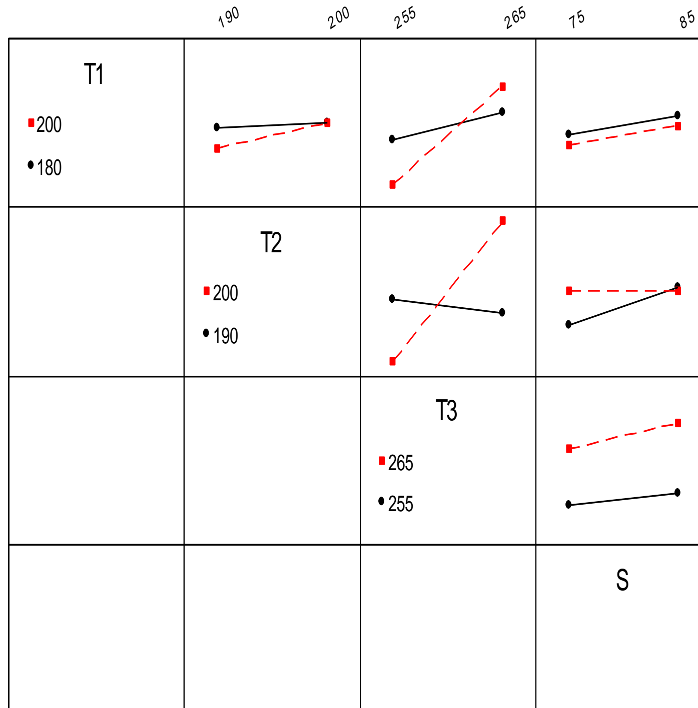

Fig 13. Interaction Diagrams

Result of Factorial Design:

The result of Full factorial design is shown in Fig 14

ISSN: 2319-5967
ISO 9001:2008 Certified
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Volume 2, Issue 3, May 2013

Six sigma

2^4 FACTORIAL DESIGN.

Estimated Effects and Coefficients for Y-AVG

Term	Effect	Coef	StDev	Coef	T	P
Constant		75.96	12.43	6.11	6.11	.002
T1	-12.50	-6.25	12.43	-0.50	-0.50	636
T2	18.58	9.29	12.43	0.75	0.75	.488
T3	71.25	35.62	12.43	2.87	2.87	035
S1	22.58	11.29	12.43	0.91	0.91	405
T1*T2	12.83	6.42	12.43	0.52	0.52	.628
T1*T3	41.00	20.50	12.43	1.65	1.65	.160
T1*S1	2.00	1.00	12.43	0.08	0.08	.939
T2*T3	83.08	41.54	12.43	3.34	3.34	.020
T2*S1	-22.42	-11.21	12.43	-0.90	-0.90	.408
T3*S1	6.42	3.21	12.43	0.26	0.26	.807

Analysis of Variance for Y-AVG

Source	DF	Seq SS	Adj SS	Adj MS	F	P
Main Effects	4	24353	24353	6088	2.46	0.175
2-Way Interactions	6	37185	37185	6197	2.51	0.166
Residual Error	5	12353	12353	2471		
Total	15	73890				

Fig 14. Result of Full Factorial Design

Regression Equation :

The regression equation is as follows

Y = 75.96 – 6.25 T1 + 9.29 T2 + 35.62 T3 + 1.29 S1 + 6.42 T1*T2 + 20.50 T1*T3
+ T1* S1 + 41.54 T2*T3 – 11.21 T2*S! + 3.21 T3*S1

Taking consideration only significant factors

Y = 75.96 + 35.82 T3 + 41.54 T2*T3

Set T2 = +1 (200°C)

Y = 75.96 + 35.82 T3 + 41.54 T3

0 = 75.96 + 77.36 T3

T3 = - 0.98

T3 = - 1.0 (Approximately)

Results of Design of Experiment:

The following are the setting for temperature profile to get optimum quality level

T1 = 180 ° C , T2 = 200 ° C , T3 = 255° C and conveyor speed ; S1 = 75 Cm/min

[ALL THESE ANALYSIS HAVE BEEN DONE USING MINITAB SOFTWARE]

V. CONCLUSION

Controller Pcbs were assembled for next eight months, all data are collated and the summary is as follows

ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 2, Issue 3, May 2013

CONFIRMATORY TESTS

OPTIMUM SET OF PARAMETERS ("X" FACTORS)

X" FACTORS	*SETTING*		*CONSTANTS*	*SETTING*
T1 °C	180		T2 °C	200
T3 °C	255		S1 (Cms/Mts)	75

DATA AFTER IMPLEMENTATION OF SIX SIGMA (PERIOD 1.07.05 To 28.02.06)

NO. OF BOARDS REFLOW SOLDERED	NO. OF OPPORTUNITIES INSPECTED	NO. OF DEFECTS	DPU	DPO	Z_{LT}	Z_{ST}
4628	26,51,844	351	0.075	$1.35e^{-4}$	**3.64**	**5.14** **(3.87)**

(Figures in brackets are for period before implementing SIX SIGMA)

Before starting of the project, the process yield was at 3.87 sigma level. In other word the process was generating 8890 defects in 1 million of opportunities. By applying six sigma techniques the process yield is improved, now defect rate is reduced to 54 defects per 1 million of opportunities.

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