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DC-DC Converter Based On Cascade Cockcroft-Walton Voltage Multiplier for High Voltage Gain without Using Transformer

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Abstract: ***This paper proposes a high step-up DC-DC converter based on Cockcroft-Walton (CW) voltage multiplier without using step up transformer. The low input DC voltage is boost up by boost inductor (L_s) in DC-DC converter and the proposed circuit performs the inverter operation. The n-stage CW-voltage multiplier is applying low input AC voltage to high output DC voltage. It provides continuous input current with low ripple, high voltage gain, reduced switching losses, low voltage stress on the switches, diodes and capacitors and also improving efficiency of the converter. The power switches having two independent frequencies f_{sm} and f_{sc}. The f_{sm} operates at higher frequency of the output voltage and it is regulated by controlling the duty cycle of S_{m1} and S_{m2}, while the f_{sc} operates at lower frequency of the desired output voltage ripple and it can be adjusted by S_{c1} and S_{c2}. Finally the proposed converter is validated by MATLAB simulation and experimental result is designed in prototype. A laboratory prototype is built for test and both simulation and experimental results demonstrate the validity of the proposed converter.***

Keywords: **Cockcroft-Walton Voltage Multiplier, High Voltage Ratio, Multilevel Inverter, Step-Up Dc-Dc Converter.**

I. INTRODUCTION

The extensive use of electrical equipment has imposed severe demands for electrical energy and this trend is constantly growing. The conventional boost DC-DC converter can provide a very high voltage gain by using an extreme high duty cycle. The step-up dc-dc converters have been proposed to obtain high voltage ratios without extreme high duty cycle by using isolated transformers or coupled inductors. The current fed converters are providing low input current ripple and high voltage ratio. Modified current-fed converters integrated with step-up transformers or coupled-inductors which focused on improving efficiency and reducing voltage stress, were presented to achieve high voltage gain without extreme high duty cycle. The design of the high-frequency transformers, coupled inductors or resonant components for these converters are relatively complex compared with the conventional boost DC-DC converter. The step-up DC-DC converters without step-up transformers and coupled inductors were presented. By cascading diode-capacitor or diode-inductor modules, these kinds of DC-DC converters provide not only high voltage gain but also simple and robust structures. The conventional Cockcroft-Walton voltage multiplier is very popular among high voltage DC applications. Replacing the step-up transformer with the boost type structure, the proposed converter provides higher voltage ratio than that of the conventional CW voltage multiplier. The proposed converter operates in continuous conduction mode, so that switch stresses, the switching loss, and EMI noise can be reduced.

The various components that are required for the construction of the high step up DC-DC converter using Cockcroft Walton voltage multiplier have been described. The AC source is supplied to diode bridge rectifier and its output is connected with DC filter to produce pure DC voltage from pulsating DC voltage. Then the DC voltage is applied to boost converter with voltage multiplier. The conventional boost DC-DC converter can provide a very high voltage gain by using an extreme high duty cycle. The step-up DC-DC converters have been proposed to obtain high voltage ratios without extreme high duty cycle by using isolated transformers or coupled inductors. The simulation details of the DC-DC boost converter using n-stage Cockcroft Walton voltage multiplier. The simulation is done by using MATLAB simulink software.

II. STEADY STATE ANALYSIS OF PROPOSED CONVERTER

The proposed converter is supplied by a low-level dc source, such as battery, PV module or fuel cell sources. The proposed converter consists of one boost inductor L_s, four switches (S_{m1}, S_{m2}, S_{c1}, and S_{c2}), and one *n*-stage CW voltage multiplier. S_{m1} (S_{c1}) and S_{m2} (S_{c2}) operate in complementary mode, and the operating frequencies of

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S_{m1} and S_{c1} are defined as f_{sm} and f_{sc}, respectively. For convenience, f_{sm} is denoted as modulation frequency and f_{sc} is denoted as alternating frequency. Theoretically, these two frequencies should be as high as possible, so that smaller inductor and capacitors can be used in this circuit. In this paper, f_{sm} is set much higher than f_{sc}, and the output voltage is regulated by controlling the duty cycle of S_{m1} and S_{m2}, while the output voltage ripple can be adjusted by f_{sc}. As shown in figure 1, the well-known CW voltage multiplier is constructed by a cascade of stages with each stage containing two capacitors and two diodes. In an *n*-stage CW voltage multiplier, there are *N* (=2*n*) capacitors and *N* diodes. For convenience, both capacitors and diodes are divided into odd group and even group according their suffixes, as denoted in figure 1.

A. Circuit Operating Principle

As shown in figure 1, the proposed converter is an integration of a boost converter with a CW voltage multiplier. The proposed converter is supplied by a low-level DC source such as battery, PV module or fuel cell sources. The proposed converter consists of one boost inductor (L_s), four switches (S_{m1}, S_{m2}, S_{c1}, and S_{c2}), and one n-stage CW voltage multiplier. S_{m1} (S_{c1}) and S_{m2} (S_{c2}) operate in complementary mode, and the operating frequencies of S_{m1} and S_{c1} are defined as f_{sm} and f_{sc}, respectively. For convenience, f_{sm} is denoted as modulation frequency and f_{sc} is denoted as alternating frequency.

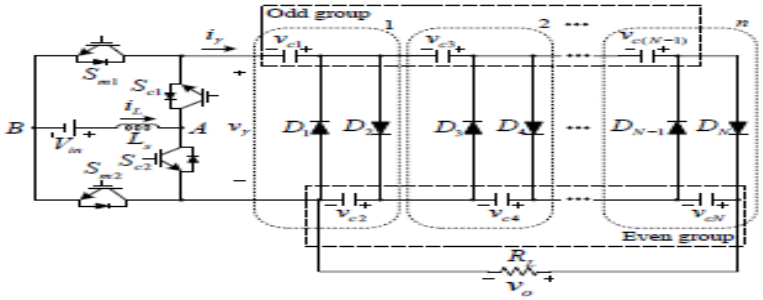


Fig1. Proposed converter with *n*-stage CW voltage multiplier

These two frequencies should be as high as possible, so that smaller inductor and capacitors can be used in this circuit. The frequency f_{sm} is set much higher than f_{sc}, and the output voltage is regulated by controlling the duty cycle of S_{m1} and S_{m2}, while the output voltage ripple can be adjusted by f_{sc}.

The circuit operation principle of the proposed converter and the characteristic behaviour of each mode in both positive and negative-half cycles are presented as follows:

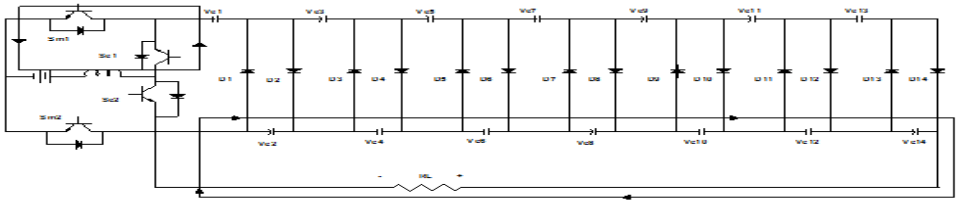
1) Mode-1: S_{m1}, S_{c1} are turned on, and S_{m2}, S_{c2}, and all CW diodes are not conducting. The boost inductor is charged by the input DC source, the odd-group of capacitors C_1, C_3, C_5, C_7, C_9, C_{11} and C_{13} are Floating, and the even-group of capacitors C_2, C_4, C_6, C_8, C_{10}, C_{12} and C_{14} are Supply the load as shown in figure 2.

2) Mode-2, 3, 4, 5, 6 & 8*:* S_{m2} and S_{c1} are turned on. S_{m1} and S_{c2} are turned off, and the current i_γ is positive. The boost inductor is discharged and input DC source transfer energy to the CW voltage multiplier through different even diodes.

Mode-2:D_{14} is Conducting and D_1 to D_{13} are not conducting, thus, the even-group capacitors C_2, C_4, C_6, C_8, C_{10}, C_8 and C_{14} - Charged and the odd-group capacitorsC_1, C_3, C_5, C_7, C_9, C_{11} and C_{13} are discharged by i_γ as shown in figure 2.

Mode-3: D_{12} is conducting, thus, C_2, C_4, C_6, C_8, C_{10} and C_{12} are charged while C_1, C_3, C_5, C_7, C_9 and C_{11} are discharged by i_γ. Simultaneously, C_{13} is supplies load current and C_{14} is floating as shown in figure 2.

Mode-4: D_{10} is conducting, thus, C_2, C_4, C_6, C_8 and C_{10} are charged while C_1, C_3, C_5, C_7& C_9 are discharged by i_γ. Simultaneously, C_{12} and C_{14} supply load current, while C_{11} and C_{13} are floating as shown in figure 2.



Mode-1

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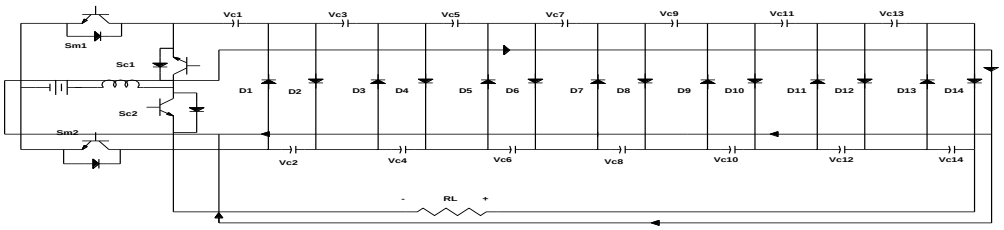
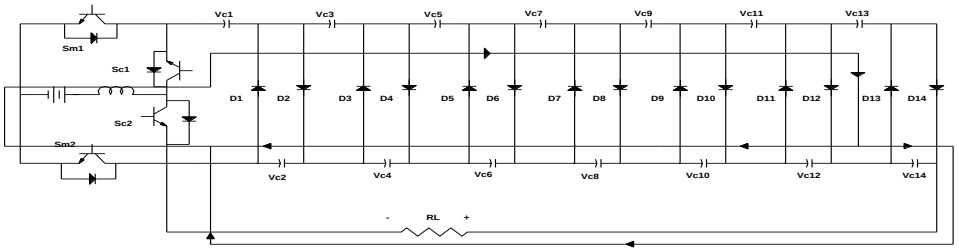
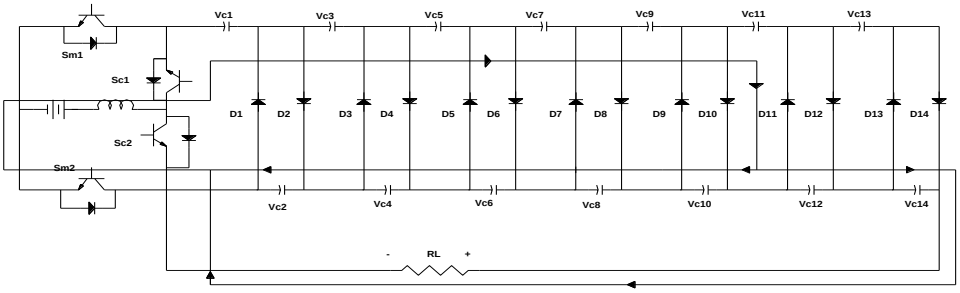


Mode-2



Mode-3



Mode-4

Mode-5: D_8 is conducting, thus, C_2, C_4, C_6 and C_8 are charged whileC_1, C_3, C_5 and C_7 are discharged by i_γ. Simultaneously, C_{10}, C_{12} and C_{14} are supplies load current and C_9, C_{11} and C_{13} are floating as shown in figure 2.

Mode-6: D_6 is conducting, thus, C_2, C_4 and C_6 are charged while C_1, C_3 and C_5 are discharged by i_γ. Simultaneously, C_8, C_{10}, C_{12} and C_{14} supply load current, while C_7, C_9, C_{11} and $C_{13}$are floating as shown in figure 2.

Mode-7: D_4 is conducting, thus,C_2 and C_4 are charged whileC_1 and C_3 are discharged by i_γ. Simultaneously, C_6, C_8, C_{10}, C_{12} and C_{14} are supplies load current and C_5, C_7, C_9, C_{11} and C_{13} are floating as shown in figure 2.

Mode-8: D_2 is conducting, thus, C_2 is charged while C_1 is discharged by i_γ. Simultaneously, C_4, C_6, C_8, C_{10}, C_{12} and C_{14} are supply load current, while C_3, C_5, C_7, C_9, C_{11} and C_{13} are floating. The behaviour of the proposed converter and CW circuit during positive-half cycle can be obtained. But, this circuit operates in forward bias condition as shown in figure 2.

3) Mode-9: S_{m2} and Sc_2 are turned on, S_{m1}, Sc_1 and all CW diodes (D_1 to D_{14}) are not conducting. The boost inductor is charged by the input DC source, the even-group capacitors C_2, C_4, C_6, C_8, C_{10}, C_{12} and C_{14} are supply the load, and the odd-group capacitors C_1, C_3, C_5, C_7, C_9, C_{11} and C_{13} are floating as shown in figure 2.

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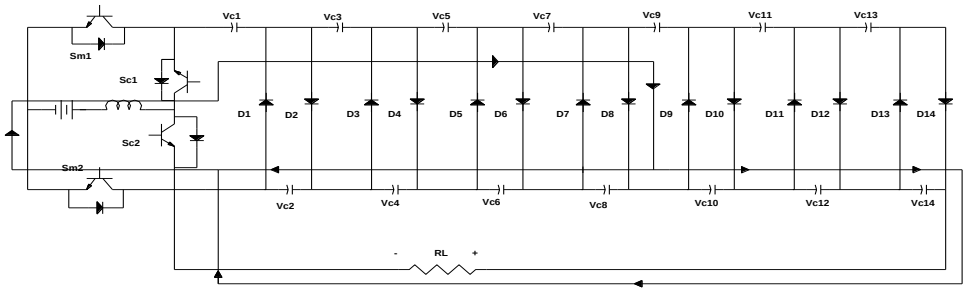
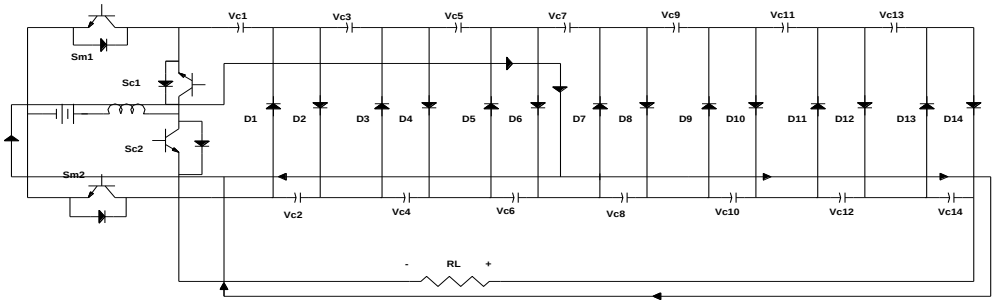
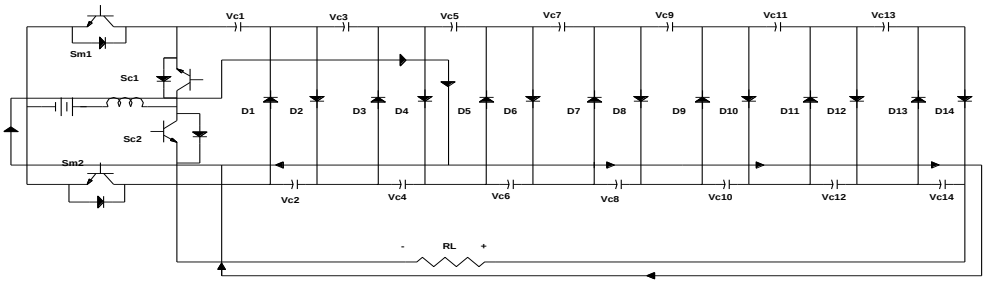


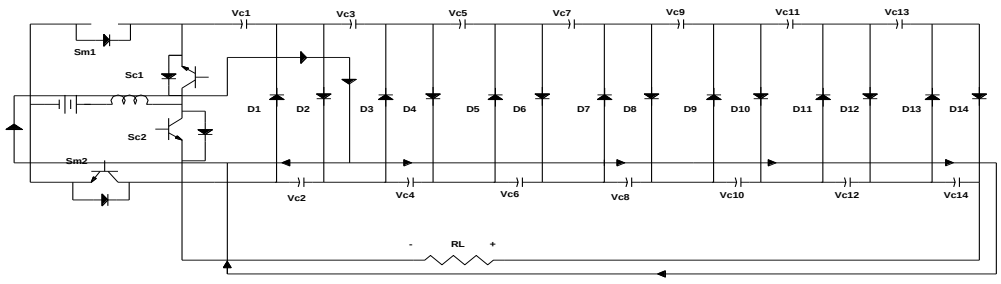
Mode-5



Mode-6



Mode-7



Mode-8

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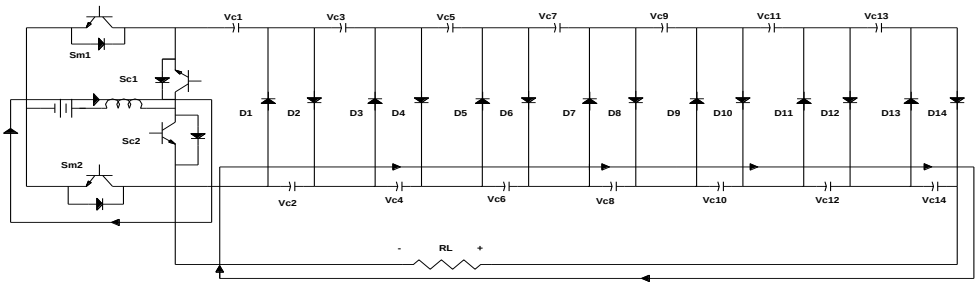
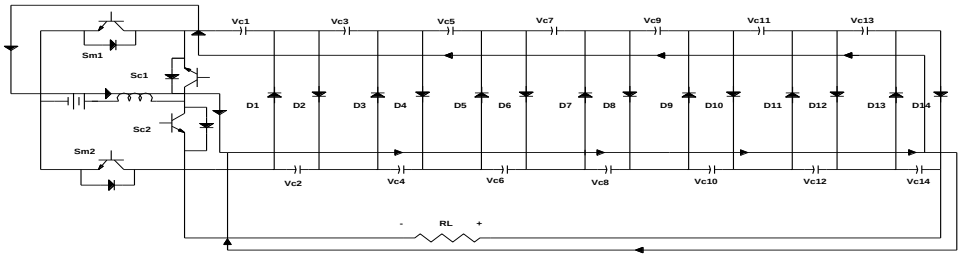


Mode-9



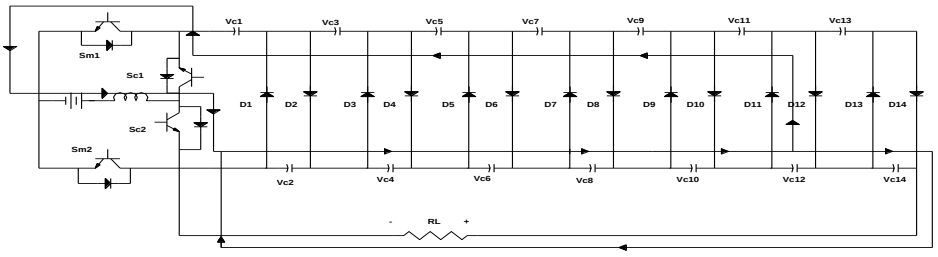
Mode-10

4) Modes-10, 11, 12, 13, 14, 15 & 16: S_{m1} and S_{c2} are turned on, S_{m2} and S_{c1} are turned off, and the current i_γ is negative. The boost inductor is discharged and input DC source transfer energy to the CW voltage multiplier through different odd diodes.

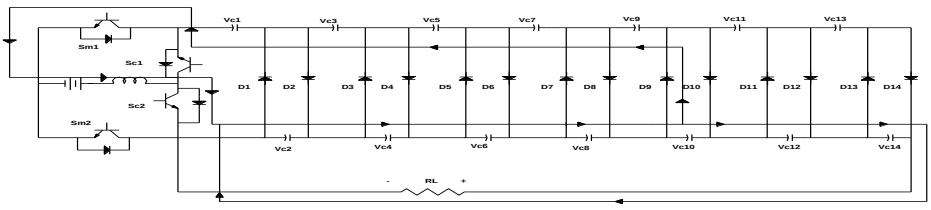
Mode-10: D_{13} is conducting, thus, the even-group capacitors C_2, C_4, C_6, C_8, C_{10}, C_{12} and C_{14} are discharged and the odd-group capacitors C_1, C_3, C_5, C_7, C_9, C_{11} and C_{13} are charged by i_γ as shown in figure 2.

Mode-11: D_{11} is conducting, thus, C_2, C_4, C_6, C_8, C_{10} and C_{12} are discharged and C_1, C_3, C_5, C_7, C_9 and C_{11} are charged by i_γ, C_{14} is supply load current and C_{13} is floating as shown in figure 2.

Mode-12: D_9 is conducting, thus, C_1, C_3, C_5, C_7 and C_9 are charged by i_γ, while all even capacitors C_2, C_4, C_6, C_8 and C_{10} are discharge, C_{12} and C_{14} are supply load current, and C_{11} and C_{13} are floating as shown in figure 2.



Mode-11



Mode-12

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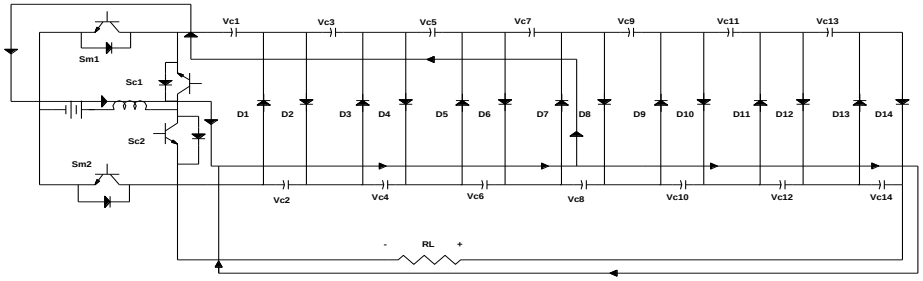
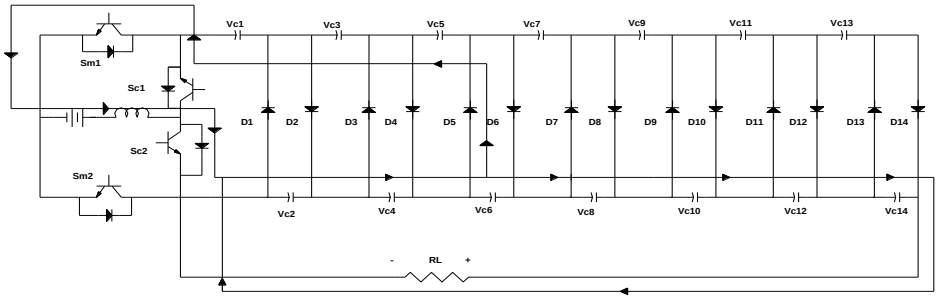
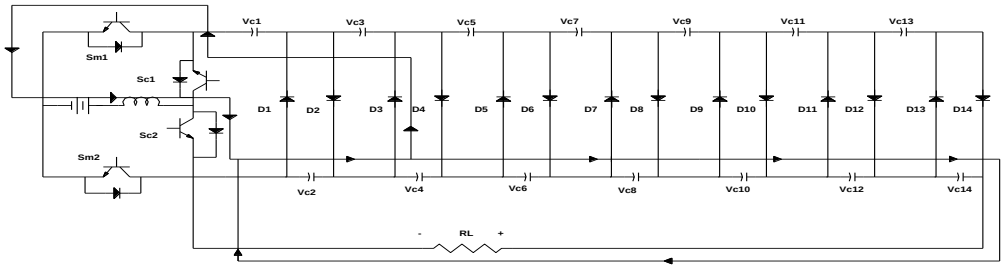


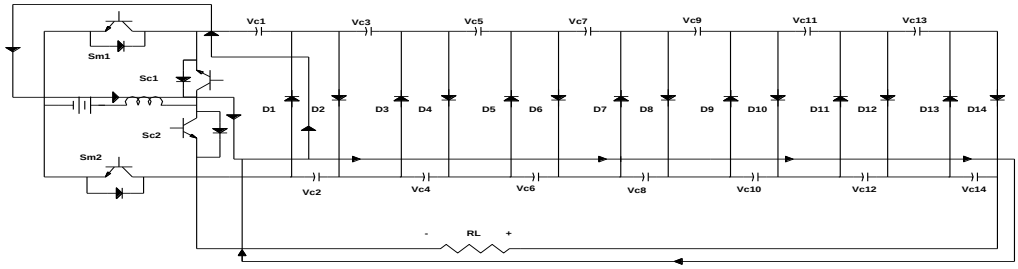
Mode-13



Mode-14



Mode-15



Mode-16

Fig 2. Conducting path of proposed converter operating modes-1 to 16.

Mode-13: D_7 is conducting, thus, C_2, C_4, C_6 and C_8 are discharged and C_1, C_3, C_5 and C_7 are charged by i_γ, C_{10}, C_{12} and C_{14} are supply load current and C_9, C_{11} and C_{13} are floating as shown in figure 2.

Mode-14:D_5 is conducting, thus, C_1, C_3 and C_5 are charged by i_γ, while all even capacitors C_2, C_4 and C_6 are Discharge, C_8, C_{10}, C_{12} and C_{14} are supply load current, and C_7, C_9, C_{11} and C_{13} are floating as shown in figure 2.

Mode-15: D_3 is conducting, thus, C_2 and C_4 are discharged and C_1 and C_3 are charged by i_γ, C_6, C_8, C_{10}, C_{12} and C_{14} are supply load current and C_5, C_7, C_9, C_{11} and C_{13} are floating as shown in figure 2.

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Mode-16: D_1 is conducting, thus, C_1 is charged by i_γ, while all even capacitors C_2 is Discharge, C_4, C_6, C_8, C_{10}, C_{12} and C_{14} are supply load current, and C_3, C_5, C_7, C_9, C_{11} and C_{13} are floating. The behaviour of the proposed converter and CW circuit during negative-half cycle can be obtained through similar process of positive-half cycle. But, it operates in reverse bias condition as shown in figure 2.

B. Cockcroft Walton Voltage Multiplier

The Cockcroft Walton (CW) voltage multiplier is constructed by a cascade of n-stage with each stage containing two capacitors and two diodes. The seven-stage CW voltage multiplier circuit diagram is shown in the figure 3. The CW-voltage multiplier having both capacitors and diodes are divided into odd group and even group according to their suffixes.

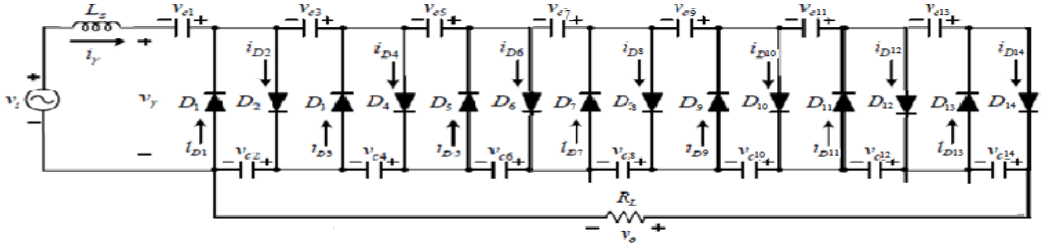

Fig 3. Seven-stage CW voltage multiplier circuit

According to the polarity of current is i_γ, the operation of the proposed converter can be divided into two parts: positive conducting interval for $i_\gamma>0$ and negative conducting interval for $i_\gamma<0$. During positive conducting interval, only one of the even diodes can conduct with the sequence D_{14}-D_{12}-D_{10}-D_8-D_6-D_4-D_2, during negative conducting interval, only one of the odd diodes can conduct with the sequence D_{13}-D_{11}-D_9-D_7-D_5-D_3-D_1. Moreover, during positive conducting interval, there are four modes of operations. In mode-1, S_{m1} turns on, thus the energy stored in the inductor increases. The switching pulse waveforms are shown in figure 4. In modes-2, 3, 4, 5, 6, 7 and 8, S_{m2} turns on, and the inductor transfers energy to the CW circuit through D_{14}, D_{12}, D_{10}, D_8, D_6, D_4, and D_2 respectively. Similarly, there are four modes of operations in the negative conducting interval (modes-9, 10, 11, 12, 13, 14, 15 and 16).

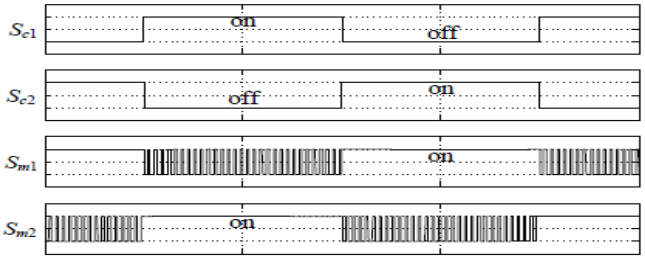

Fig 4. Switching pulse waveforms

III. SIMULATION CIRCUIT

The simulation circuit is separated in to two parts; they are DC-DC boost converter with inverter and seven stages of Cockcroft Walton voltage multiplier circuit. The proposed converter is supplied by a low-level DC source such as battery, PV module or fuel cell sources. The simulation circuit of proposed converter with seven-stage CW voltage multiplier is shown in figure5. The proposed converter consists of one boost inductor L_s, four switches (S_{m1}, S_{m2}, S_{c1}, and S_{c2}) and one n-stage CW voltage multiplier. S_{m1} (S_{c1}) and S_{m2} (S_{c2}) operate in complementary mode, and the operating frequencies of S_{m1} and S_{c1} are defined as f_{sm} and f_{sc}, respectively. For convenience, f_{sm} is denoted as modulation frequency and f_{sc} is denoted as alternating frequency

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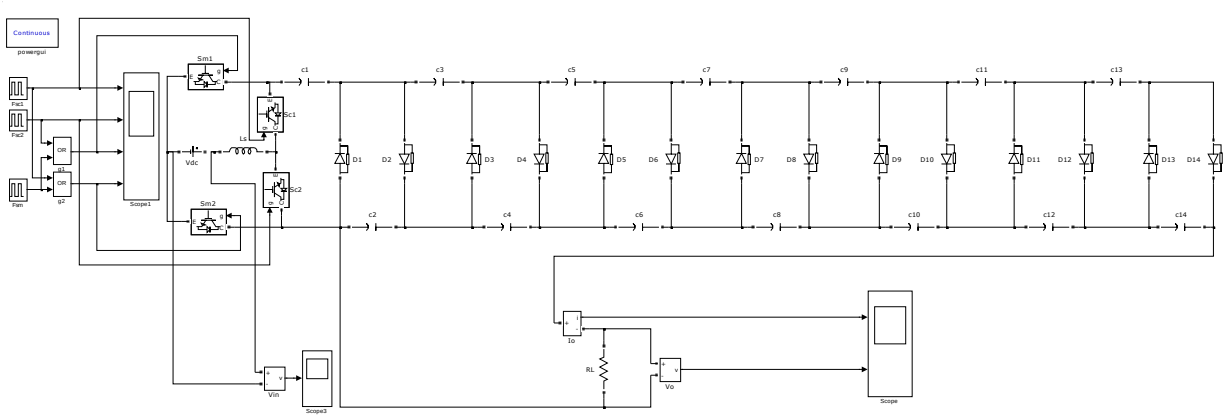

Fig 5.Simulation circuit of proposed converter with seven-stage CW voltage multiplier.

These two frequencies should be as high as possible, so that smaller inductor and capacitors can be used in this circuit. The frequency f_{sm} (60 kHz) is set much higher than f_{sc} (1 kHz), and the output voltage is regulated by controlling the duty cycle of S_{m1} and S_{m2}, while the output voltage ripple can be adjusted by f_{sc} in S_{c1} and S_{c2}. The system specification of the prototype designs is shown in table I. The Cockcroft Walton voltage multiplier is constructed by a cascade of n-stages with each stage containing two capacitors and two diodes. The CW-voltage multiplier having both capacitors and diodes are divided into odd group and even group.

IV. DESIGN CONSIDERATIONS OF PROPOSED CONVERTER

In this section, the voltage and current stresses on each capacitor, switch, and diode will be considered. Moreover, the values of inductor and capacitors will be discussed as well.

A. Capacitor Voltage Stress

In steady-state condition, assuming that all capacitors are large enough, then each capacitor in an n-stage CW voltage multiplier, theoretically it has the same voltage except the first one, which has one half of the others. As a result, the maximum voltage stress on each capacitor is $V_{o,pk}/n$, except that the first one is $V_{o,pk}/2n$, where $V_{o,pk}$ is the maximum peak value of output voltage. For comparison, the voltage stress on each capacitor corresponding to the high step-up converters. It can be seen that the capacitor voltage of the proposed converter only depends on the input voltage and duty cycle, while the capacitor voltages of the others are dependent on the number of the cascade stages, thus the determination of the capacitor rating is easier for the proposed converter.

B. Capacitance of CW-Voltage Multiplier

A major advantage of the conventional CW voltage multiplier is that the voltage gain is theoretically proportional to the number of cascaded stages. In previous section, the ideal voltage gain (unloaded) is assumed to simplify the circuit analysis. Unfortunately, when a load is connected to the load side of the system, the voltage drop and ripple across on each capacitor cannot be ignored. For an n-stage CW voltage multiplier, the output voltage is equal to the total voltage of all even capacitors, the output voltage of proposed converter cascaded with Cockcroft Walton voltage multiplier can be expressed as

Vo = nVc

Where, V_0 is output voltage, n is number of stages of CW-voltage multiplier, V_C is voltage across the even capacitor. Thus the simulation of proposed boost converter with seven-stage CW voltage multiplier is done by using MATLAB simulink software.

V. SIMULATION RESULTS AND WAVEFORM ANALYSIS

A prototype was built to verify the validity of the proposed converter. The system specifications and the waveform explain in detail the operation of proposed DC-DC boost converter with seven-stage Cockcroft Walton voltage multiplier. Components of the prototype are summarized in table I and table II, respectively. Moreover, Matlab/Simulink is applied to simulate the mathematic model and control strategy of the proposed converter. Some selected waveforms of the proposed converter at V_{in}=48V, ŋ=93.5%and V_o=1.05kV for both simulation and experiment. The upper part of the switching signals having four switches, in which S_{c1} and S_{c2} are operated at f_{sc}, and S_{m1} and S_{m2} are operated at f_{sm}. Moreover, the simulation results of the output voltage v_o, the input current i_L, the terminal voltage v_γ and current i_γ of the CW voltage multiplier are shown in the lower

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part. The experimental waveforms of the switching signals, v_o, i_L, v_γ, and i_γ. Obviously, the simulation results well agree with experimental results. A prototype with corresponding rating was built to verify the validity of the proposed converter. Moreover, the MATLAB Simulink is applied to simulate the mathematic model and the control strategy of the proposed converter.

Table 1: System Specification of the Prototype

Parameters	**Ratings**
Input DC voltage, V_{in}	42-54 V
Output Voltage, V_o	1.05 KV
Modulation frequency, f_{sm}	60 kHz
Alternating frequency, f_{sc}	1 kHz
Resistive load, R_L	1 Kω
Stage numbers, n	7
Boost inductor, L_s	1.5 mH
Capacitors, C_1 - C_2	470 µF

TABLE II .Component List for the Prototype

Components Description	**Symbol**	**Value/Part no.**
Control IC	-	ICE1PCS01
CPLD	-	LC4256V
Boost inductor	L_s	1.5mH
Power switches	S_{m1}, S_{m2}, S_{c1}, S_{c2}	IRF640
Capacitors	$C_1 – C_2$	470µF/400V
Diodes	$D_1 – D_2$	SF20L60U
Gate driver	-	HCPL-3120

A. Simulation and Experimental Results

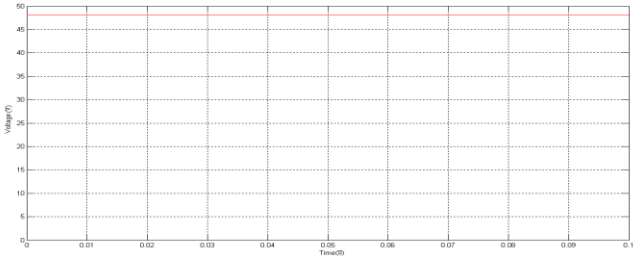

Fig 6. Simulation of boost converter of DC input voltage waveform

The output waveform of the boost converter of DC input voltage is shown in figure 6.Some selected waveforms of the proposed converter V_{in}=48V, and V_o=1.05kV for both simulation and experiment. The upper part of the switching signals of simulation for the four switches, which $S_{c1}$and S_{c2} are operated at f_{sc}, and S_{m1} and S_{m2} are operated at f_{sm}. The simulation results of the output voltage v_o, the input current i_L, the terminal voltage v_γ and terminal current i_γ of the CW voltage multiplier are shown in the lower part of the experimental waveforms of the switching signals such as v_o, i_L, v_γ, and i_γ.

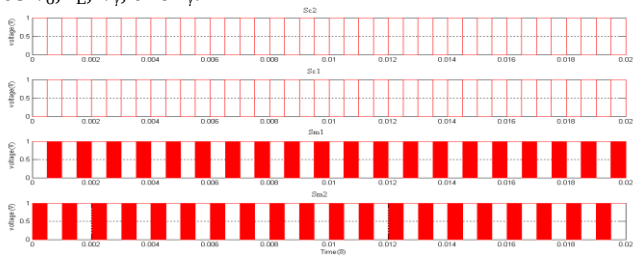

Fig 7. Simulation of gate switching pulse waveforms

The simulation of switching pulse waveforms in DC-DC boost converter is shown in figure7.Obviously, the simulation results well agree with experimental results. In theoretical analysis, the input current ripple frequency (f_{sc}) is ignored due to that the capacitors are assumed large enough to obtain stable capacitor voltages with no voltage ripple in the CW voltage multiplier. However, the voltage ripple exists practically in all capacitors. In other words, the input current and the output voltage have the same ripple frequency (f_{sc}).The simulation of output voltage waveform is shown in figure 8.

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The results also influence the terminal voltage V_γ and current i_γ of the CW voltage multiplier. The efficiency of the proposed converter with different input voltages are 42 V to 54 V. The output voltage of the proposed converter is regulated at 1.05 kV.

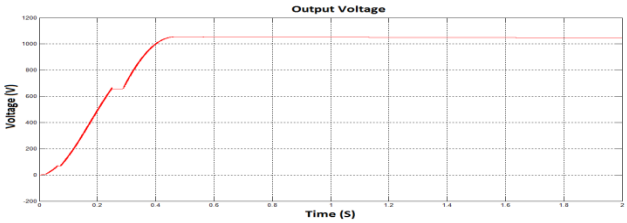

Fig 8. Simulation of output voltage waveform

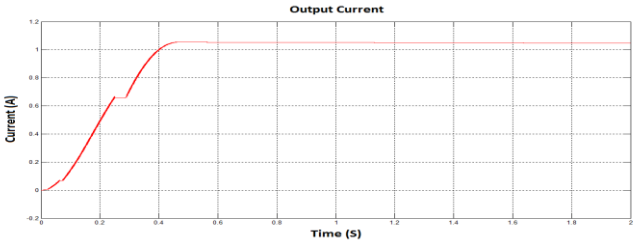

Fig 9. Simulation of output current waveform

The results represent that the proposed converter has lower efficiency at lower input because of higher conducting loss accompanied by higher input current. On the other hand, for higher load condition, the efficiency decreases due to the conducting loss of the diodes and the resistance loss of the capacitors. The highest system efficiency for these three input voltages appears at output power (P_o) load. A maximum 93.15% efficiency is achieved at 48 V input voltage. Finally, the theoretical, simulated, and experimental voltage gains under V_{in}=48 V, R_L=1 kΩ, f_{sc}=1 kHz, f_{sm}=60 kHz. Seven different stages (n=1 to 7) of CW circuit were used, while the experimental results demonstrate only for n=1 to 7 The efficiency of the proposed converter with different input voltages are 42V, 48V and 54V. The output voltage of the proposed converter is regulated at 1.05kV, thus, the voltage gains corresponding to these three input voltages are 10.7, 9.4 and 8.3, respectively. The simulation of output current waveform is shown in figure 9. The results represent that the proposed converter has lower efficiency at lower input because of higher conducting loss accompanied by higher input current. On the other hand, for higher load condition, the efficiency decreases due to the conducting loss of the diodes and the resistance loss of the capacitors. The highest system efficiency for these three input voltages appears at depends load. A maximum 93.15% efficiency is achieved at 54V input voltage. The reason is that the effect of the parasitic elements increases when the proposed converter operates under high duty cycle, and the voltage gain will be deteriorated. The proposed converter still can provide high voltage gain without extreme high duty cycle. Thus the simulation of the DC-DC boost converter using Cockcroft Walton voltage multiplier was successfully carried out using MATLAB simulink software and the output waveforms were observed.

VI. CONCLUSION

In this paper, a high step-up DC-DC converter based on CW voltage multiplier without a line or high-frequency step-up transformer was presented to obtain a high voltage gain. Since the voltage stress on the active switches, diodes, and capacitors is not affected by the number of cascaded stages, power components with same voltage ratings can be selected. The mathematical modeling, circuit operation, design considerations, and control strategy were discussed. The control strategy of the proposed converter can be easily implemented with a commercial average-current-control and continuous current mode with adding a programmed. The proposed control strategy employs two independent frequencies, one of which operates at high frequency to minimize the size of the inductor, while the other one operates at relatively low frequency according to the desired output voltage ripple. Finally, the simulation and experimental results proved the validity of theoretical analysis and the feasibility of the proposed converter. In future work, the influence of loading on the output voltage of the proposed converter will be derived for completing the steady-state analysis. Thus the design, simulation and analysis of proposed DC-DC boost converter with seven-stage Cockcroft Walton voltage multiplier was done.

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