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Power Efficient Counter Design Using Conditional Pulse Enhancement Flip-Flop

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Abstract-Flip-flops is critical timing elements in digital circuits which have a large impact on the circuit speed and power consumption. The performance of flip-flop is an important element to determine the efficiency of the whole synchronous circuit. In an attempt to reduce power consumption in flip-flops a pulse enhancement method is presented. An implicit type pulse triggered flip-flop is designed using conditional pulse enhancement scheme. The pulse generation logic use two input AND gate at its discharge path which reduces the circuit complexity and hence the overall power is reduced. Pulses that trigger discharging are generated only when there is a need, so unwanted circuit activity due to glitches can be avoided which reduces the overall power consumption. Pulse discharge can be made faster. The delay inverters which consume more power for stretching the pulse width are replaced by the PMOS transistors which enhances the pull down strength when there is a longer discharge path. Transistor sizes are also reduced to provide area and power saving. Johnson counters which provide glitch free decoding can be designed with such flip-flops. As a result power consumption can be reduced compared to conventional methods.

I. INTRODUCTION

The increasing prominence of portable systems and the need to limit power consumption (and hence, heat dissipation) in very-high density Very Large Scale Integration (VLSI) chips have led to rapid and innovative developments in low-power design during the recent years. Increasing chip density and higher operating speed lead to the design of very complex chips with high clock frequencies. Typically, the power dissipation of the chip and the temperature increases linearly with the clock frequency. Architecture-level measures include smart power management of various system blocks, utilization of pipelining and parallelism, and design of bus structures. Finally, the power consumed by the system can be reduced by a proper selection of the data processing algorithms, specifically to minimize the number of switching events for a given task. Circuit-level measures such as the proper choice of circuit design styles, reduction of the voltage swing and clocking strategies can be used to reduce power dissipation at the transistor level. Flip-flops are the basic storage elements used to store one bit data. They are extensively used in all sequential designs. Nowadays in order to speed up the task, several pipelining techniques are used. These techniques mainly use flip-flops. Extensive power is consumed by the clock circuitry. About 20%-30% of the total system power is consumed by the clock distribution circuit itself. The main reason for such extensive power consumptions is that the clock pulses have 100% transitions. On the other hand the logic circuit consumes only little power because the pulse transitions are very less compared to clock transitions. Conventional master slave flip-flops have two separate clocks for the master and slave and hence consume more power. A delay is introduced between the input and the output which provides the expected results but comparatively slower. Edge-Triggered flip-flops consume more power. Performance of the system is a major concern and the need for high speed circuits have increased. High speed in the sense it needs high clock frequency for its operation which in turn consumes more power.

In the VLSI design nowadays, the clocking system and interconnections alone consume about 20% to 40% of the total chip power. It is important to reduce the clocking system power. So we go for low-power designs. One idea is to reduce clock voltage swing, requires four clock lines, which will increase clock interconnection capacitance. Moreover, routing four clock lines is disadvantageous in area and the phase adjustment is difficult [2]. For high speed applications, the flip-flop should have a simple clocking scheme. True Single phase Clocking serves that purpose but it has longer latency [3]. The clock power is also increased due to the use of more storage elements due to several pipeline stages. In order to achieve high performance, power efficient designs are necessary. One approach is to use dual-edge clocking. But precisely control the arrival of both clock edges is difficult [5]. Traditional master-slave flip-flops are made up of two stages, one master and one slave and they are characterized by their hard-edge property. Alternatively, pulse-triggered flip-flops reduce the two stages into one stage and are characterized by the soft edge property. The logic complexity and number of stages inside these pulse-triggered flip-flops are reduced, leading to small D-to- Q delays. One of the main advantages of pulse-triggered flip-flops is that they allow time borrowing across cycle boundaries as a result of the zero or

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even negative setup time [8].Power dissipation can be reduced by reducing unwanted switching state inside the circuits. Energy recovery circuits achieve low energy dissipation by restricting current to flow across devices with low voltage drop and by recycling the energy stored on their capacitors by using an ac-type (oscillating) supply voltage [4]. But energy recovery in storage elements is not possible. There are several techniques like conditional precharge, conditional discharge and conditional capture to reduce switching power [8].Gating of clocks reduce power to a great extent. But there is some delay overhead. The clock inverter is skewed for fast high-to-low transitions, the conducting period occur only during the rising transition of the clock, but not on the falling transition. In this way, an implicit conducting pulse is generated during each rising transition of the clock. A cascade of three inverters instead of one can give a slightly sharper falling edge for the inverted clock (CLKB).

Pulse triggered flip-flops can be used for low power operation. The term pulse-triggered means that data are entered into the flip-flop on the rising edge of the clock pulse, but the output does not reflect the input state until the falling edge of the clock pulse. Pulse triggered flip-flops are sensitive to any change of the input levels during the clock pulse is still HIGH, the inputs must be set up prior to the clock pulse's rising edge and must not be changed before the falling edge. There is a need of only one latch, so circuit complexity is reduced. Pulse triggered flip-flops are less sensitive to clock skew and jitter. They reduce the two stages in the master slave flip-flop into one stage and are characterized by the soft edge property. The logic complexity and number of stages inside these pulse-triggered flip-flops are reduced, leading to small D -to- Q delays. One of the main advantages of pulse-triggered flip-flop is that they allow time borrowing across cycle boundaries as a result of the zero or even negative setup time. Due to these timing issues, pulse-triggered flip-flops provide higher performance than their master-slave counterparts. It needs pulse generation logic for generating the control pulse.

Depending on the type of pulse generation, the flip-flop can be classified into implicit type and explicit type. Explicit type flip-flop requires additional circuitry for pulse generation as the pulse trains are generated physically. The pulse generator can be shared by the neighboring flip-flops. It is energy efficient. It consumes more power for operating the circuit and hence not suitable for low power significant designs. Also due to the presence of large capacitive loads at the output i.e. if a pulse generator drives many number of flip-flops, the problem becomes more significant. It also has some pulse width control issues on applying low power techniques like conditional capture, conditional precharge, conditional discharge or conditional data mapping. Implicit type flip-flops do not have separate pulse generation logic. The logic is designed along with the flip-flop. So there is no need for additional circuit for pulse generation and the power consumption is reduced. It is a power efficient design. But due to the presence of longer discharge paths it has some inferior timing characteristics. On applying certain low power techniques the timing characteristics become very worse. So there is a need to enlarge the transistor sizes to produce wider pulses to trigger the data capturing of the flip-flops.

A Johnson counter (or switch tail ring counter, twisted-ring counter, walking-ring counter) is a modified ring counter, where the output from the last stage is inverted and fed back as input to the first stage. The register cycles through a sequence of bit-patterns, whose length is equal to twice the length of the shift register, continuing indefinitely? These counters find specialist applications, including those similar to the decade counter, digital-to-analog conversion, etc. They can be implemented easily using implicit type D flip-flops that results in reduced power consumption. In the VLSI design nowadays, the clocking system and interconnections alone consume about 20% to 40% of the total chip power. It is important to reduce the clocking system power. So we go for low-power designs. One idea is to reduce clock voltage swing, requires four clock lines, which will increase clock interconnection capacitance. Moreover, routing four clock lines is disadvantageous in area and the phase adjustment is difficult [2]. For high speed applications, the flip-flop should have a simple clocking scheme. True Single phase Clocking serves that purpose but it has longer latency [3]. The clock power is also increased due to the use of more storage elements due to several pipeline stages. In order to achieve high performance, power efficient designs are necessary. One approach is to use dual-edge clocking. But precisely control the arrival of both clock edges is difficult [5]. Traditional master-slave flip-flops are made up of two stages, one master and one slave and they are characterized by their hard-edge property. Alternatively, pulse-triggered flip-flops reduce the two stages into one stage and are characterized by the soft edge property. The logic complexity and number of stages inside these pulse-triggered flip-flops are reduced, leading to small D-to-Q delays. One of the main advantages of pulse-triggered flip-flops is that they allow time borrowing across cycle boundaries as a result of the zero or even negative setup time [8].Power dissipation can be reduced by reducing unwanted switching state inside the circuits. Energy recovery circuits achieve low energy dissipation

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by restricting current to flow across devices with low voltage drop and by recycling the energy stored on their capacitors by using an ac-type (oscillating) supply voltage [4]. But energy recovery in storage elements is not possible. There are several techniques like conditional precharge, conditional discharge and conditional capture to reduce switching power [8].Gating of clocks reduce power to a great extent. But there is some delay overhead. The clock inverter is skewed for fast high-to-low transitions, the conducting period occur only during the rising transition of the clock, but not on the falling transition. In this way, an implicit conducting pulse is generated during each rising transition of the clock. A cascade of three inverters instead of one can give a slightly sharper falling edge for the inverted clock (CLKB).

II. IMPLICIT-TYPE P-FF DESIGN WITH PULSE CONTROL SCHEME

A. ip-DCO (implicit pulsed-Data Close to Output)

There are many implicit type pulse triggered flip-flop designs. These designs inherit various other designs to show low power consumption. The ip-DCO is an efficient design, is given in Fig 1(a). The pulse generator is AND based logic and a semi-dynamic structured latch design which can interface both dynamic and static structures. Implementing logic designs are easy and delay penalty is small. It occupies small area and also it uses single phase clocking. It has Inverters I5 and I6 are used to latch data and inverters I7 and I8 are used to hold the internal node. The complementary of the clock signal is taken and it is delay skewed and applied as the input to the pulse generator to generate a transparent window equal in size to the delay by inverters I1-I3. There are two disadvantages. It has larger switching power and there is a larger capacitance load which causes speed and performance degradation.

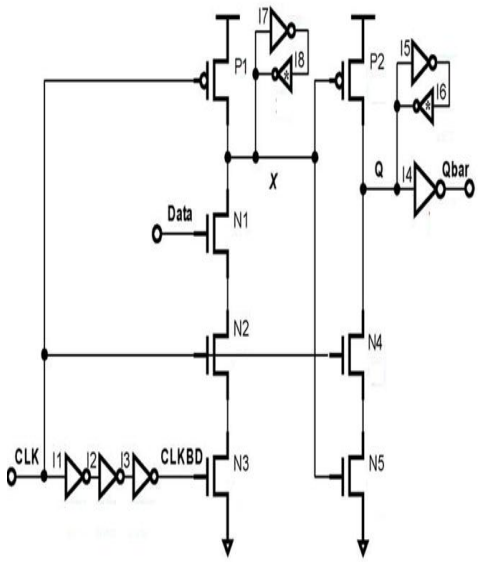

Fig 1(a). Ip-DCO

B. MHLLF (Modified Hybrid Latch Flip-flop)

MHLLF is a modified and improved P-FF design Fig.2 Static latch structure is employed. Precharging of the node reduces the delay, but the power consumption is increased. Here the periodical precharging of node by the clock signal does not take place. When Q is low, the node is maintained high with the help of a weak pull-up transistor P1 which is controlled by the FF output signal Q. The unnecessary discharging problem at node is eliminated by using this design. But during the "0" to "1" transition, there is a longer Data-to-Q. This is mainly because node is not pre-discharged. The area consumption is high because we need larger transistors to enhance the discharging capability. When D=Q=1 there is extra power consumption because of the floating nodes.

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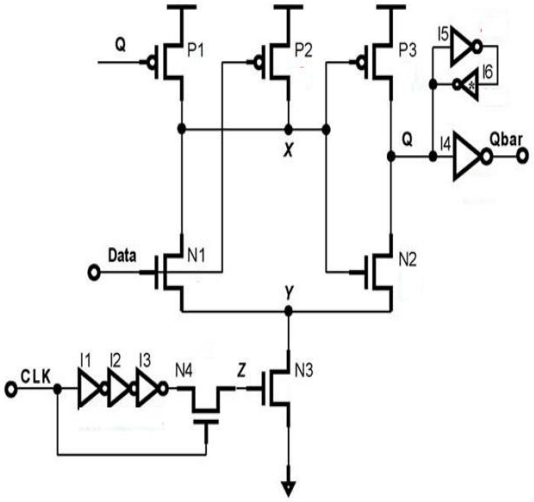

Fig 2. MHLLF

C. SCCER (Single Ended Conditional Capture Energy Recovery)

SCCER is a design which is a modification over the ip-DCO design. It uses a conditional discharged technique in which the discharge path is controlled by eliminating the switching activity when the input stays in stable HIGH. In this design, the back to back inverters which is used instead of pull up and pull down resistors is replaced by a weak pull up transistor P1 and inverter I2 to reduce the load capacitance of node. The series connection of two nMOS transistors N1 and N2 is used in the discharge path. An extra nMOS transistor N3 is used to eliminate the unwanted switching activity. The Q_fdbk is used to control N3, so if D=1 there is no discharge. The discharge path is long when the input data is "1". It takes place through four transistors i.e., N1 through N4, while battling with the pull up transistor P1. In this case, we need a powerful pull-down circuitry to ensure that the node can be properly discharged. This pull-down circuit needs additional area and power. As the area increases, the discharge path takes longer time which increases the delay. There is also a need for a wider pulse width to perform the discharge operation.

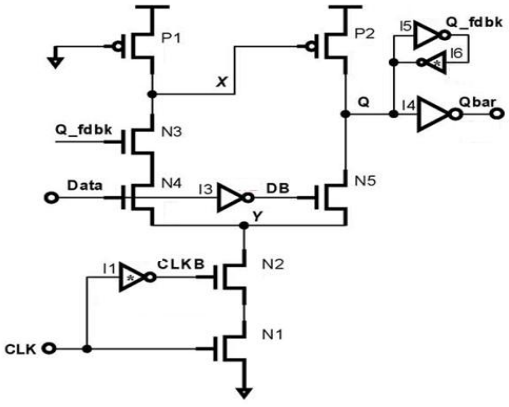

Fig 3. SCCER

D. P-FF Design with conditional pulse enhancement scheme

There are two measures employed to overcome the draw backs in the conventional designs. Due to the presence of the large number of transistors in the discharge path the delay is high and also large power is consumed in power-up of the transistors. So, the number of nMOS transistors in the discharging path should be reduced. There is a need to increase the pull down strength when the input D=1. So there is a need to conditionally enhance the pull down strength when input data is "1." This design inherits the upper part of the SCCER design. Transistor stacking design in Fig. 1 and 3, is replaced by removing the transistor N2 from the discharging path.

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Transistor N2 and N3 are connected in parallel to form a two-input pass transistor logic (PTL)-based AND. It controls the discharge of transistor N1. The input to the AND logic is always complementary to each other. As a result, the output node is kept at zero most of the time. There is a floating node when both input signals equal to "0". But it doesn't provide any harm to the circuit performance. The critical circumstance occurs only when there is rising edges at the clock pulse. Transistors N2 and N3 are turned ON together in this case to pass a weak logic high to node. This weak pulse strength is enhanced by switching ON the transistor N1 by a time span equal to the delay provided by inverter I1. The switching power at node can be reduced due to a diminished voltage swing. Unlike the MHLLF design, where the discharge control signal is driven by a single transistor, parallel conduction of two nMOS transistors (N2 and N3) speeds up the operations of pulse generation. On designing the flip-flop in this way, the number of transistors in the discharging path can be reduced. This speeds up the pulse generation and hence delay is reduced. The area overhead is also reduced.

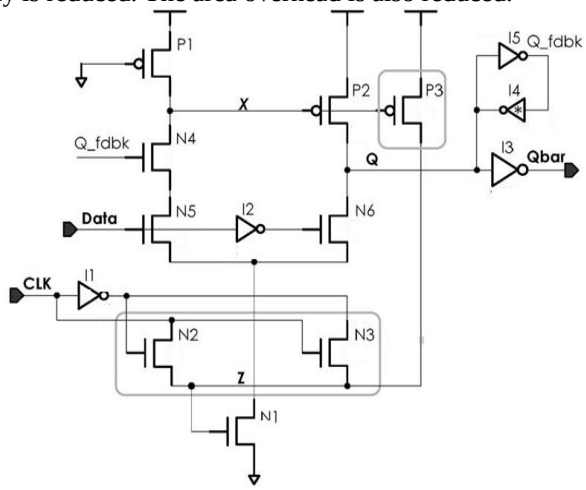
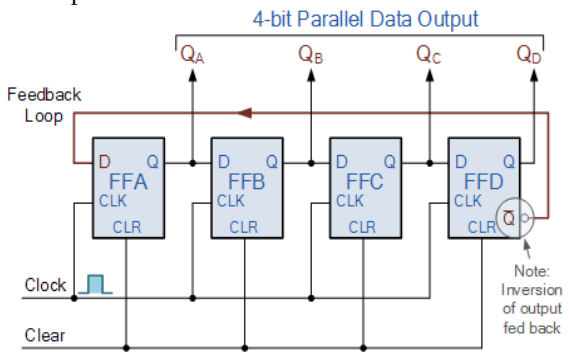


Fig 4. ***P-FF Design with conditional pulse enhancement scheme***

III. JOHNSON COUNTER USING FLIP-FLOP DESIGNS

Flip-flops are the basic storage elements and can be used to design registers, counters and memory elements. By designing a Johnson counter using such designs, we can prove that the counter designed with pulse enhancement scheme provides low power consumption in the counters.



IV. SIMULATION RESULTS

The design is simulated using Micro wind software. The average power consumed is calculated. The power consumption varies for different frequencies. For any frequency, the pulse enhancement flip-flop shows reduced power consumption compared to other designs. A simulation window appears with inputs and output. The power consumption is also shown on the right bottom portion of the window. Generate the layout again and run the simulations till you achieve your target delays. Depending on the input sequences assigned at the input the output is observed in the simulation. These designs include the three P-FF designs shown in Fig. 1 (ip-DCO , MHLLF , SCCER) and another Pulse triggered –Flip-Flop design called conditional capture FF (CCFF).

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V. CONCLUSION

In this paper, the various Flip-flop design like, ip-DCO, MHLLF and SCCER are discussed. The comparison table also added to verify the designed methods. With these all results pulse enhancement scheme performed better than ip-DCO, MHLLF and SCCER designs. The counter designed with all these flip-flop designs also prove that pulse enhancement scheme is a better low power design.

Table.1.Power Consumed By Various Flip-Flops at Different Frequencies

FREQUENCY (Hz)	ip-DCO (MicroWatts)	MHLFF (MicroWatts)	SCCER (MicroWatts)	CPES (Micro Watts)
100 M	649	522	334	85.651
500 M	617	527	336	84.889
1 G	619	535	339	84.427
1.25 G	624	535	340	87.667
2 G	634	546	345	88.846
2.5 G	**641**	**549**	**348**	**92.312**
3 G	649	559	350	91.641
5G	681	587	390	92.011
10 G	743	641	445	113
20 G	852	746	449	139

Table 2.Power Consumed By Johnson Counters at F=2.5 Ghz

FREQUENCY (Hz)	ip-DCO (MilliWatts)	MHLFF (Milli Watts)	SCCER (MilliWatts)	CPES (Milli Watts)
2.5 G	2.602	1.824	1.541	0.494

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