



ISSN: 2319-5967

ISO 9001:2008 Certified

International Journal of Engineering Science and Innovative Technology (IJESIT)

Volume 2, Issue 2, March 2013

Design and Implementation of Low-Power High-Speed Full Adder cell using GDI Technique

T. Divya Bharathi, B.N. Srinivasa Rao
Dept., of ECE, AIET. Visakhapatnam

Abstract – Full custom implementation is used to develop digital circuits in new technology to achieve high performance low power and area efficient designs. In this paper, The low power and high performance 1-bit full adder cell is proposed. The modified Gate Diffusion Input (GDI) technique has been used for generation of XOR and CARRY functions. Fifteen states of the arts 1-bit full adders and one proposed full adder are simulated with TSPICE using 0.18 μ m CMOS Technology at 1.8v supply voltage. The resulting full adder circuit is realized using of the 18 transistors, while having full voltage-swing in all circuit nodes. By optimizing the transistor size in each stage the power and delay are minimized. The results of post-layout simulation compared to similar reported ones illustrate significant improvement. Simulation results show great improvement in terms of Power-Delay-Product.

Index Terms — Low-power, High-speed, Full custom, full adder, GDI Technique.

INTRODUCTION

Full Adder Cell plays a vital role in Digital Signal Processors (DSPs), Application Specific ICs (ASICs), Digital Processors etc., Increasing the performance of 1-bit full adder shows a great impact on increasing the performance of the whole system. Hence the realisation of full adders with low power and high performance is very essential. VLSI designers have used speed as the performance metric. In general, small area and high performance are two conflicting constraints [1]. The power consumed for any given function in CMOS circuit must be reduced for either of the two different reasons: One of these reasons is to reduce heat dissipation in order to allow a large density of functions to be incorporated on an IC chip. Any amount of power dissipation is worthwhile as long as it doesn't degrade overall circuit performance. The other reason is to save energy in battery operated instruments same as electronic watches where average power is in microwatts. In CMOS circuits, the power consumption is proportional to switching activity, capacitive loading and the square of the supply voltage [2]. Full Adder is one of the most important parts of each processor, which is used in floating-point, in the arithmetic logic unit (ALU), digital signal processing, image, video processing, and microprocessors and in all the arithmetic operations such as division, multiplication, subtraction. Increasing the performance of a 1-bit Full Adder cell is very effective in increasing the Performance of the whole system [3]. The structure of the rest of this paper is organized as follows: Section II reviews fifteen states of the full adder cells. In section III the Implementation of full adder with the modified GDI Technique is described. The simulation results are shown in section IV. Finally, section V contains the conclusion.

REVIEW OF FOURTEEN STATE OF THE ART FULL ADDER CELLS

There are different types of CMOS full adder. this section reviewed the fourteen states of the arts 1-bit full adders. This proposed cell is compared with them. Fourteen state of the art full adder cells are: 10T, 14T, CPL, TFA, TG CMOS, C²MOS, Hybrid, Bridge, FA24T, N-Cell, DPL, Mod2f, HPSC and TSAC. The first full adder structure in this section is 10T. It has only 10 transistors. The number of transistors is the advantage of this cell which leads to better performance and less silicon area. However poor driving capability and non full swing nodes are the serious problems of this full adder cell. The power consumption of this structure is 1.13 μ w. It is shown in figure 1(a). The 14T adder with 14 transistors consumes considerably less power in the order of microwatts and has higher speed. The 14T adder reduces threshold loss problem compared to the previous different types of transistor adders. In future, this kind of low power and high speed adder cell will be used in designing the digital FIR filter and its applications in various fields. The power consumption of this structure is 6.4 μ w. It is shown in figure 1(b) [4]. The Complementary Pass-transistor Logic (CPL) full adder is shown in figure 1(c). This is contains the 18 transistors that based on NMOS pass-transistor network. This causes low input capacitance and high speed operation. Due to



ISSN: 2319-5967

ISO 9001:2008 Certified

International Journal of Engineering Science and Innovative Technology (IJESIT)

Volume 2, Issue 2, March 2013

less output voltage swing that is the result of one V_t loss in the output, CPL consumes less power than standard static CMOS circuits. The power consumption of this structure is $2.5\mu\text{w}$ [4].

A Transmission Function Full Adder (TFA) based on the transmission function theory is shown in figure 1(d). It has 16 transistors. The power consumption of this structure is $12\mu\text{w}$. A Transmission- Gate Adder (TGA) is shown in figure 1(e). Transmission gate logic circuit is a special kind of pass-transistor logic circuit. It is built by connecting a PMOS transistor and an NMOS transistor in parallel, which are controlled by complementary control signals. Both the PMOS and NMOS transistors will provide the path to the input logic "1" or "0", respectively when they are turned on simultaneously. Thus, there is no voltage drop problem whether the "1" or "0" is passed through it. It contains the 20 transistors [5]. The Complementary CMOS full adder ($C^2\text{MOS}$) is shown in figure 1(f). The advantage of complementary CMOS style is its robustness against voltage scaling and transistor sizing which are essential to provide reliable operation at low voltage and arbitrary transistor. It contains the 28 transistors [5]. Hybrid Full Adder cell, which contains the 26 transistors, utilizes a modified low-power XOR/XNOR circuit. In this circuit worst case delay problems of transitions from 01 to 00 and from 10 to 11 are solved by adding two series PMOS and two series NMOS transistors respectively. The power consumption of this structure is $2.22\mu\text{w}$. It is shown in figure 1(g) [4].

The Bridge circuit has 26 transistors which is shown in figure 1(h). This design creates a conditional conjunction between two circuit nodes. Since one of the important parameters in circuit design is the chip area, the proposed style might reduce the area or increase density of transistors in this unit of area. The power consumption of this structure is $1.66\mu\text{w}$ [6].

The FA24T structure is shown in figure 1(i). This full Adder is based on Bridge style. FA24T has 24 transistors. The body of FA24T has two transistors less than Bridge and has better power consumption. However, in FA24T the Sum generator should wait to receive the Cout signal from the Cout generator; therefore, the delay of FA24T is more than Bridge. The power consumption of this structure is $1.66\mu\text{w}$ [4].

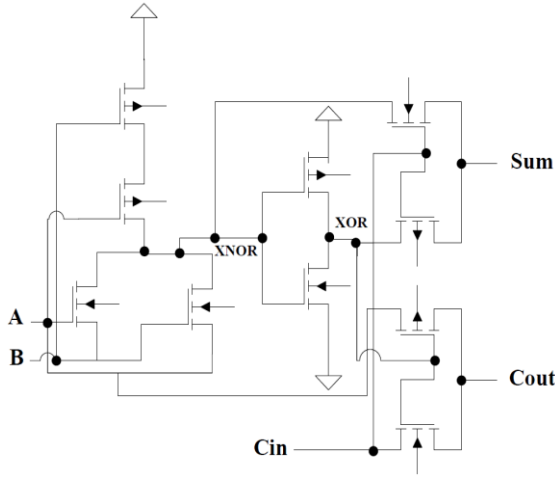
N-CELL contains the 14 transistors and utilizes the low power XOR/XNOR circuit. There is a pass transistors network to produce a non full swing Sum signal and uses four transistors to generate a full swing Cout signal. However, NCELL Full Adder cell has 12 transistors less and better performance in comparison with Hybrid Full Adder cell. The power consumption of this structure is $1.62\mu\text{w}$. It is shown in figure 1(j) [4].

The Double Pass-transistor Logic (DPL) Full Adder of the figure 1(k) is a modified version of CPL and contains the 24 transistors. Full swing operation is obtained by simply adding PMOS transistors in parallel with the NMOS transistors in DPL circuits. Therefore, the problems of little noise margin and performance degradation at low supply voltages, which occur in CPL circuits because of the output voltage drop, are avoided. However, the addition of PMOS transistors bring about increased input capacitances. The power consumption of this structure is $2.35\mu\text{w}$ [4].

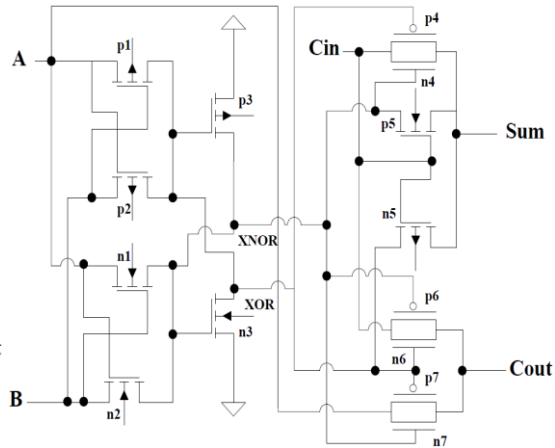
Mod2f Full Adder cell of Figure 1(l), which contains the 14 transistors, generates full swing XOR and XNOR signals by utilizing a pass transistor based DCVS circuit. As mentioned in, this leads to higher speed and better performance in comparison with the circuit proposed. The power consumption of this structure is $2.23\mu\text{w}$ [4].

The HPSC is based on feedback logic, as shown in Figure 1(m). HPSC has a feedback connection between XOR and XNOR function eliminating the non-full- swing operation. The existence of VDD and GND connections give good driving capability to the circuit and the elimination of direct connections between them and avoid the short circuit currents component. There is a delay in switching the feedback transistors. This occurs because of one of the feedback transistors which is switched ON by a weak signal and the other signal is at high impedance state. It contains the 22 transistors and the power consumption of this structure is $0.25\mu\text{w}$ [7].

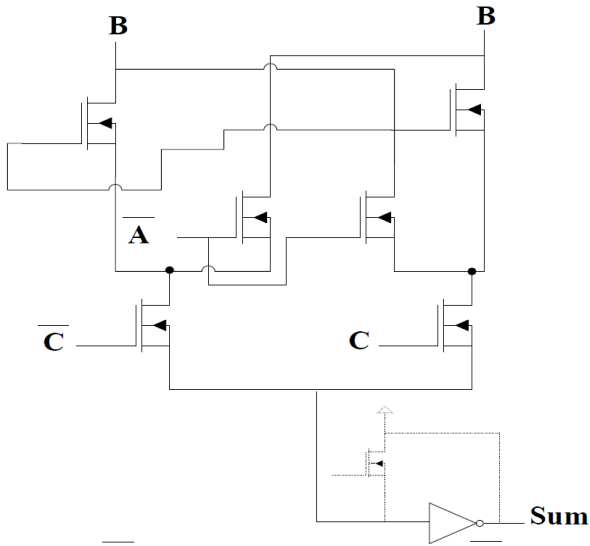
he TSAC full adder of Figure 1(n) is based on the c2mos logic style. This circuit has inherited the advantages of c2mos logic style, which has been proved in to be superior in performance to all pass transistor logic style for all logic gates except XOR at high supply voltage. It contains the 26 transistors [7].



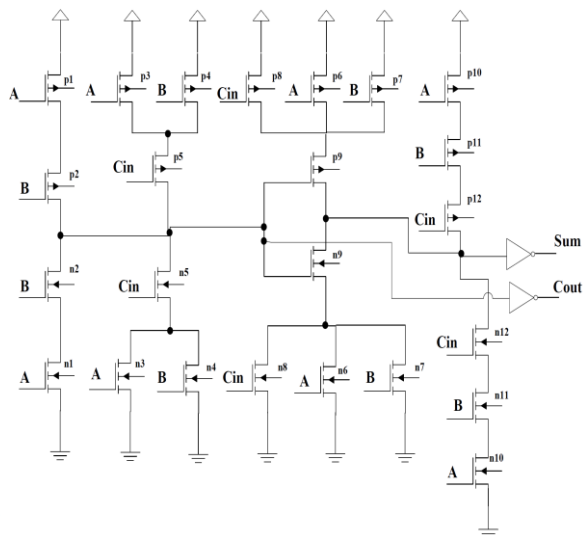
(1-a)



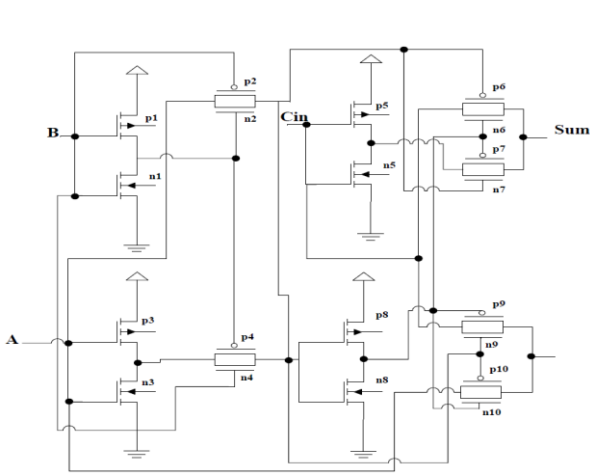
(1-b)



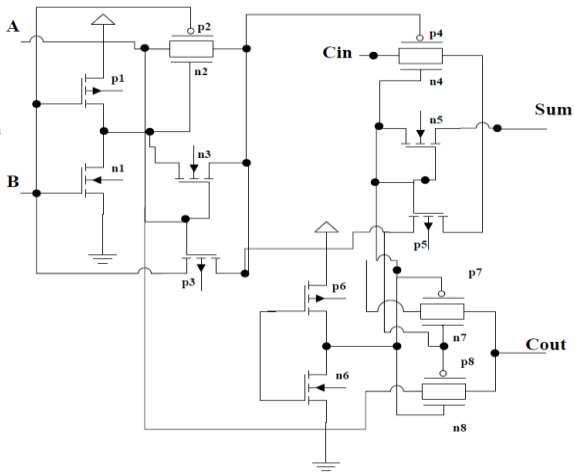
(1-c)



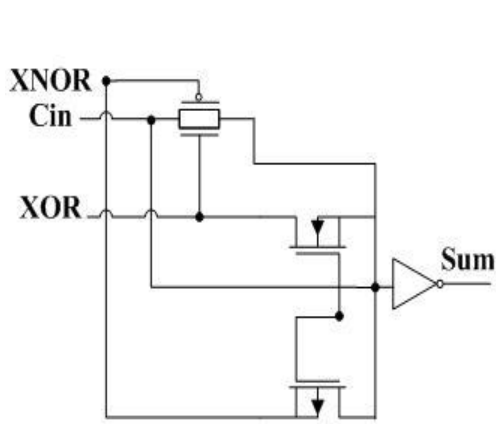
(1-d)



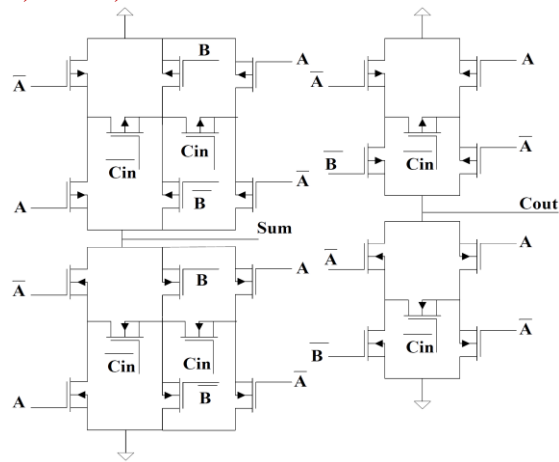
(1-e)



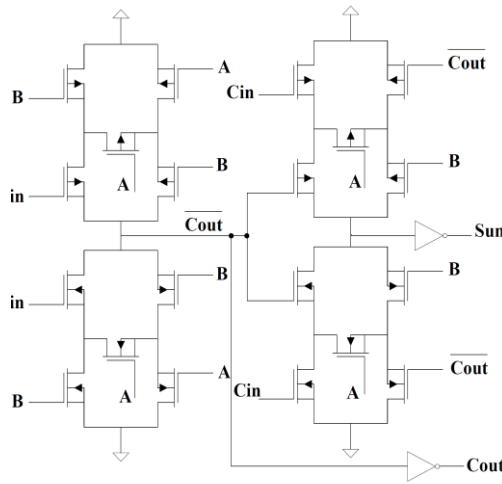
(1-f)



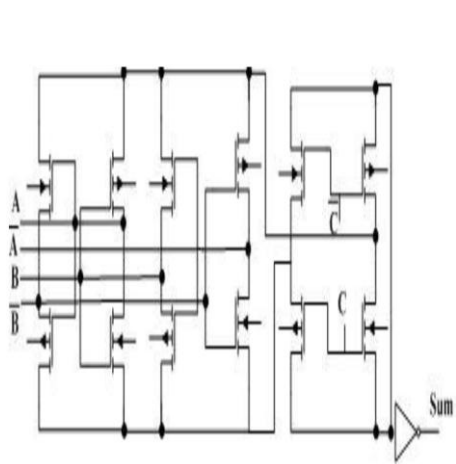
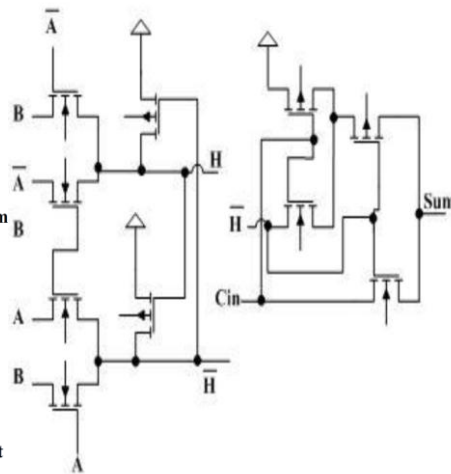
(1-g)



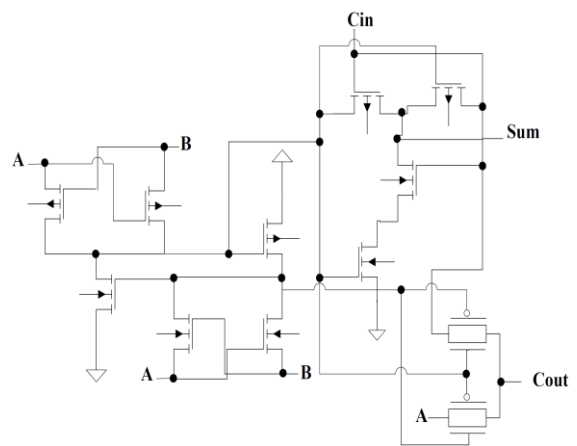
(1-h)

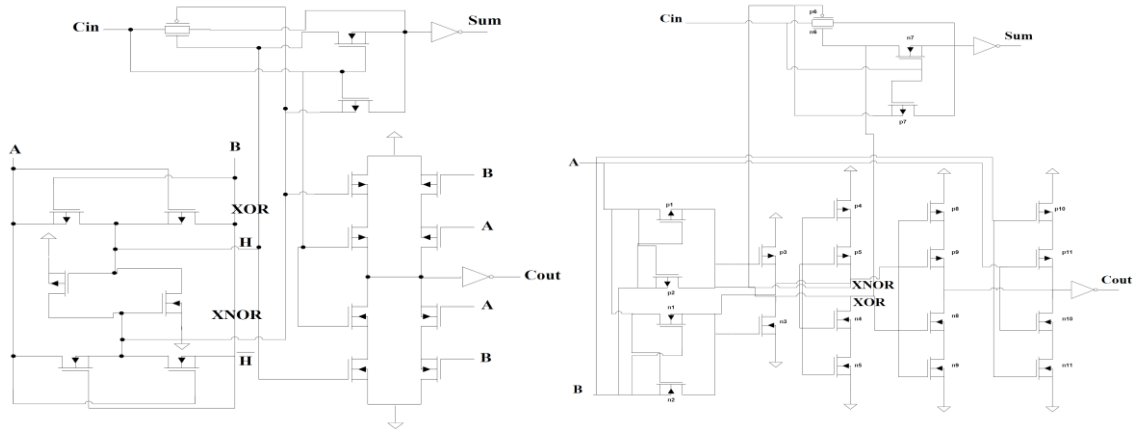


(1-i) &(1-j)

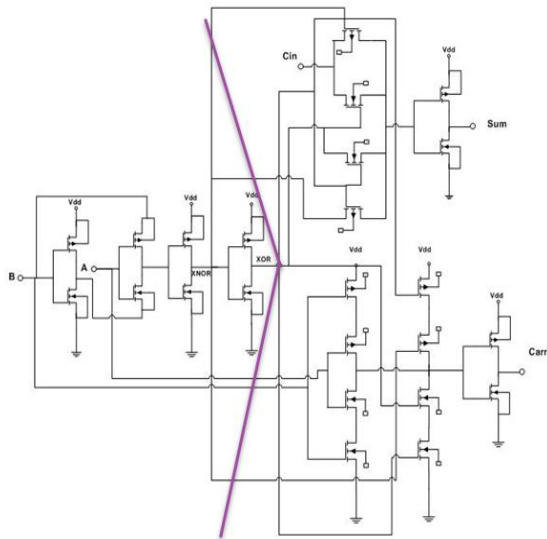


(1-k) &(1-l)





(1-m) & (1-n)



(1-o)

Fig.1- Fifteen state of the art full adder cells .(a)10T, (b)14T, (c)CPL, (d)TFA, (e)TG-Cmos, (f)C2mos, (g)Hybrid, (h)Bridge, (i)FA24T, (j)N-Cell, (k)DPL, (l)Mod2f, (m)HPSC, (n)TSAC,(o)FA-GDI.

The GDI full adder cell has the 24 transistors that is shown in figure.(1-o). This cell provides 0.78 μ W and 50ns delay.

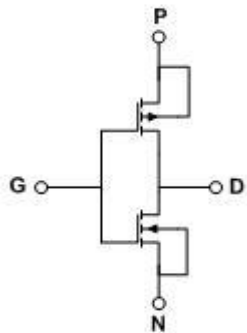


Fig. 2- GDI basic cell

III. MODIFIED GDI TECHNIQUE AND IMPLEMENTING OF FULL ADDER CELL

Gate-Diffusion-Input (GDI) method is based on the use of a simple cell as shown in figure .2. At a first glance the basic cell reminds the standard CMOS inverter, but there are some important differences:

- 1) GDI cell contains three inputs – G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of NMOS).
 - 2) Bulks of both NMOS and PMOS are connected to N or P respectively, so it can be arbitrarily biased at contrast with CMOS inverter. It must be remarked, that not all the functions are possible in standard P-Well CMOS process, but can be successfully implemented in Twin-Well CMOS or SOI technologies [8].
- ut the modified GDI cell is shown in figure.3 can be implemented in N-Well CMOS Technology by connecting Bulks of NMOS and PMOS to GND and VDD respectively. Here, when ever the P and N terminals are connected to logic ‘0’ and logic ‘1’ respectively, we should not use GND and VDD. We need to generated logic ‘0’ and logic ‘1’ signals separately and can be connected.

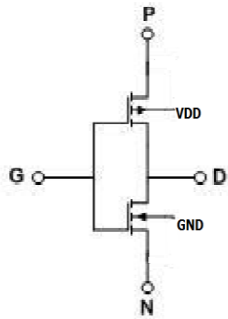


Fig. 3- Modified GDI basic cell

N	P	G	D
'0'	B	A	A'B
B	'1'	A	A'+B
'1'	B	A	A+B
B	'0'	A	AB
C	B	A	A'B+AC
'0'	'1'	A	A'

Table I: Some logic functions that can be implemented with a single GDI cell

Table I shows how a simple change of the input configuration of the simple GDI cell corresponds to very different Boolean functions. Most of these functions are complex (6-12 transistors) in CMOS, as well as in standard PTL implementations, but very simple (only 2 transistors per function) in GDI design method. OR function is the key variable in adder equation. If the generation of it is optimized, this could greatly enhance the performance of the full adder cell. In this new cell has used the modified GDI technique for generating of XOR function. It uses only six transistors to generate the XOR function the goal of this paper is to design a high performance and low power full adder cell with the GDI technique. The full adder cell has the 18 transistors that is shown in figure.4. In the first stage of this cell, the modified GDI technique is used for generating XOR functions. This stage shows full swing with low voltage. The Sum and Carry outputs are generated from the first stage. Since adder cells are normally cascaded to form a usual arithmetic circuit and their capabilities must be ensured. The proposed full-adder cell schematic and layout are shown in the figure 4(a) and 4(b) respectively.

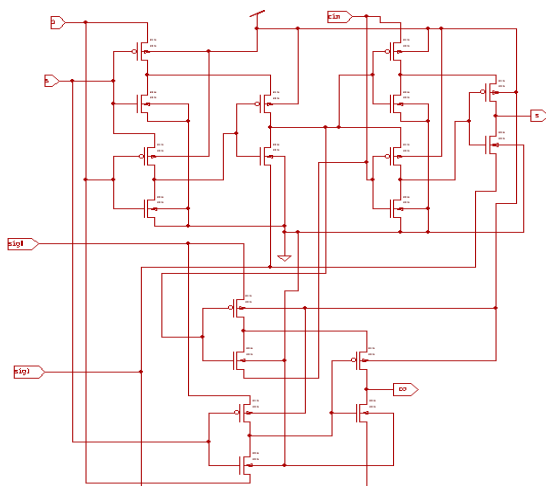


Fig. 4(a)- The proposed full adder cell with modified GDI technique

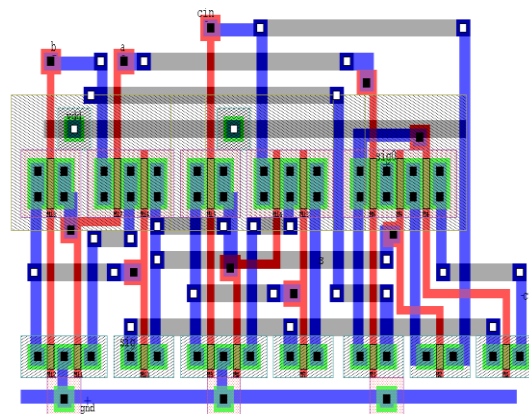


Fig. 4(b)- The full adder



ISSN: 2319-5967

ISO 9001:2008 Certified

International Journal of Engineering Science and Innovative Technology (IJESIT)

Volume 2, Issue 2, March 2013

IV.SIMULATION DETAILS

The simulation results show the actual delay of the full adder operation. In this all the timing delays are extracted. The power consumption also find from the post lay out simulation. The comparisons shown in the table. TANNER Tool used for design implementation and for simulation. have achieved in sizes that the circuit has an accurate operation. Simulation results are performed by PSPICE based on 0.18µm CMOS technology. The power supply is 1.8v. In the table II, comparison of similar works and their results have been there. The snapshot of the waveforms at 1.8v is shown in figure 5.

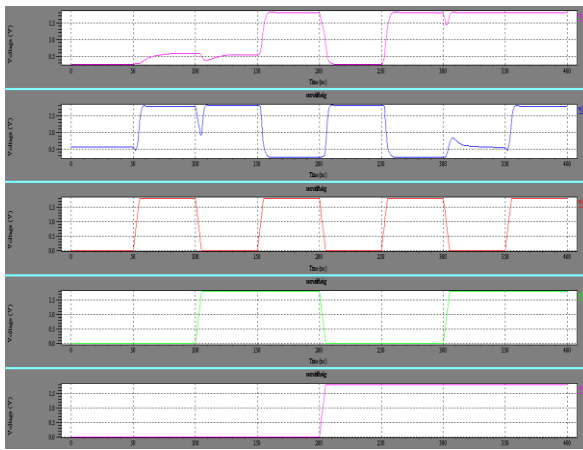


Fig.5- Snapshots of waveforms at 1.8v

Structure	No. Transistors	Power (µw)	Delay (ns)	PDP (aj)
10T	10	1.13	73.5	83.05
14T	14	6.4	-	-
CPL	18	2.5	141.1	352.7
TFA	16	12	-	-
TGA	20	-	342	-
C2MOS	28	-	364	-
HYBRID	26	2.22	80.6	178.9
FA24T	24	1.66	137.9	228.9
BRIDGE	26	1.66	104.2	172.9
N-CELL	14	1.62	63.2	102.3
DPL	24	2.35	75.3	176.9
MOD2F	26	2.23	87.7	195.5
HPSC	22	0.25	141	35.25
TSAC	26	-	128	-
FA-GDI	24	0.78	50	39
This work	18	.135(nW)	1.68	-

Table.2 comparison of similar works (Power, Delay and Power-Delay-Product)

V. CONCLUSION

The aim of this work is two have been power reduction and speed increase in the full adder. In this operation the GDI technique was introduced. By using techniques such as size optimizing in full adder could reduce the power consumption. As a result, the full adder works at the 10 MHz speed with 0.138 nW power consumption. These results were obtained with spice simulation from the extracted net list of the layouts for normal parameters, room temperature and power supply at 1.8v.

ACKNOWLEDGMENT

This material is based upon work supported by the students of Avanthi Institute of Engineering and Technology. Any opinions, findings, conclusions or recommendations expressed in this material are those of the authors and do not necessarily react the views of AIET.

REFERENCES

- [1] Rabaey J.M., A. Chandrakasan, B.Nikolic, “Digital Integrated Circuits, A Design” 2nd 2002, prentice Hall, Englewood Cliffs, NJ.
- [2] A. M. Shams, T. K. Darwish and M. A. Bayoumi. “Performance Analysis of Low Power 1-Bit CMOS full adder cells”, IEEE Transaction on VLSI Systems, Vol. 10, Feb. 2002.
- [3] K.Navi, M.R.Saatchi, O.Daei, “A high speed hybrid full Adder”, European journal of scientific research.vol.26, No.1, 2009.
- [4] M.Moaiyeri, R. Faghieh Mirzaee, K.Navi, “Two New Low Power and High Performance Full Adders”, Journal of Computers, Vol. 4, No. 2, February 2009.
- [5] C. H. Chang, J. Gu and M. Zhang, “A review of 0.18µm full adder performance for tree structured arithmetic circuits”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 13, No. 6, pp.686- 695, June 2005



ISSN: 2319-5967

ISO 9001:2008 Certified

International Journal of Engineering Science and Innovative Technology (IJESIT)

Volume 2, Issue 2, March 2013

- [6] K. Navi, O. Kavehei, M. Ruholamini, A. Sahafi, Sh. Mehrabi and N. Dadkhahi , “Low power and High Performance 1-Bit CMOS Full Adder Cell”, Journal of Computers, Vol. 3, No. 2, February 2008.
- [7] Young. Woon Kim, Hae. Jun Seo, Tae.Won Cho, “A Design of High Speed 1-Bit Full Adder Cell using 0.18 μm Cmos Process”, Proceeding of The 23rd International Technical Conference on Circuits/Systems, Computers and communications, ITC-CSCC 2008.
- [8] A.R, Saberkari, SH. Shokouhi, “A Novel Low-Power-Voltage Cmos 1-Bit Full Adder Cell with the GDI Technique”, Proceeding of The 2006 IJME-INTERTECH conference.
- [9] A.Bazzazi and B. Eskafi, “Design and Implementation of Full Adder Cell with the GDI Technique Based on 0.18 μm CMOS Technology”, Proceedings of the International Multiconference of Engineers and Computer Scientists 2010 vol II, IMECS 2010, March 17-19,Hong Kong.

AUTHORS PROFILE



T. Divya Bharathi was born in Vijayanagaram, Andhra Pradesh, India. She has received her B.Tech degree in Electronics and Communication Engineering from Jawaharlal Nehru Technological University, Kakinada, India and pursuing M. Tech in VLSI System Design from Jawaharlal Nehru Technological University, Kakinada, India. Currently she is a student in Avanthi Institute of Engineering and Technology Makavarapalem, Visakhapatnam, Andhra Pradesh, India. Her area of interests VLSI Full-Custom design.



B.N. Srinivasa rao received his B.Tech degree in Electronics and Communication Engineering from JNT University, Hyderabad, India and M.Tech in VLSI System Design from JNT University, Hyderabad, India. He is currently working as an Assistant Professor in Avanthi Institute of Engineering and Technology, Visakhapatnam, Andhra Pradesh, India. He has 5 years teaching and 9 years industrial experience. He has 7 publications in various International conferences. His area of interest VLSI Semi and full custom design. He guided many projects for B.Tech and M.Tech students.