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A Novel Data Storage Technique by Converting 2^N*N Memory bits into a N-bit Synchronous Counter

Mohsin khan.A[1], C P Latha[2], Ghouse Ahamed Z[3], Fazlulla Khan[4]
[1, 2, 3, 4] Dept of Electronics & Communication, HMSIT, Tumkur, Karnataka

***Abstract*---This paper presents a novel non-volatile data storage technique in which a $2^N * N$ memory bits are converted to a simple N-bit synchronous counter which holds the complete information of $2^N * N$ memory bits in the form of its count, by drastically reducing the huge size of memory required for storing corrupt free information and also increases the data access speed. The proposed method can make a revolution in data storage technology.**

***Index Terms*---Memory, Counter, Data Storage, Non-volatile.**

I. INTRODUCTION

A data storage memory holds the information which may be permanent (Non-Volatile) or temporary (Volatile).Every day the requirement of data storage memories is increasing and there is a huge demand for robust, corrupt free, small size, portable, fast and cheap memories for permanent storage of information either for long term or short term. As we know it is possible to design combinational circuits for any logical expression and counters with any needed counting sequence [1]--[4]. In this paper a novel technique for non volatile data storage is proposed which is robust, corrupt free, small in size, faster and very cheap in which huge information can be stored by just converting it to a simple synchronous counter. i.e. $2^N * N$ Memory bits are converted to a simple N-bit synchronous counter which holds the complete information of $2^N * N$ memory bits in the form of needed counting sequence. Example- A 4GB of data can be converted to a 32-bit synchronous counter. This can be extracted back by powering and connecting the appropriate clock signal to the counter in which every count gives 32-bits of information which can be read with the speed of clock frequency connected to the counter. Different data access speeds can be achieved by varying the clock frequency of the counter.

II. SYSTEM DESIGN

The step by step procedure for converting $2^N * N$ memory bits to a simple N-bit synchronous counter is as follows.

- A matrix1 of $2^N * N$ memory bits is taken which is to be stored (converted to an N-bit synchronous counter).
- The $2^N * N$ memory bits are segmented into N-bits each and stored in a matrix2, which holds N-bits of information in each row.
- A synchronous N-bit counter is designed to generate the exact binary information which is stored in the matrix2 of step2.
- Once the counter design is completed. It holds the complete information of $2^N * N$ memory bits in the form of its count.
- The information from the counter can be extracted back by connecting to the power supply and appropriate clock signal whose frequency matches with the read frequency. Every count of the counter gives N-bit information finally generating $2^N * N$ memory bits of information after 2^N clock cycles.

Example:

The Table-I shows the matrix1 of 2^4 *4 memory bits and Table-II shows a matrix2 holding 4-bits segment in each Row. This is constructed from matrix1.

A 4-bit synchronous counter is designed to count the sequence exactly matching with the sequence present in the matrix2 of Table-II by using 4-bit up-counter with combinational circuit designed for the truth table shown in Table-III. The block diagram of final circuit is shown in fig.1, which holds the complete 64-bits information of matrix1 in the form of 4-bit count. Which can be extracted back by giving 2^4 clock cycles.

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Table-I: Matrix of 2^4*4 memory bits.

Matrix1 =

1 1 0 1 0 1 1 1
1 1 0 0 1 1 0 0
0 0 1 1 0 1 1 1
1 1 1 0 0 1 0 1
1 1 0 0 1 1 0 0
0 0 1 1 0 1 1 1
1 1 1 0 0 1 0 1
0 0 1 1 0 1 1 1

1 1 0 1 → 1st 4-bit segment

Table-II: Segmented Matrix of 2^4*4 memory bits.

Matrix2 =

1 1 0 1
0 1 1 1
1 1 0 0
1 1 0 0
0 0 1 1
0 1 1 1
1 1 1 0
0 1 0 1
1 1 0 0
1 1 0 0
0 0 1 1
0 1 1 1
1 1 1 0
0 1 0 1
0 0 1 1
0 1 1 1

Table-III: Truth table

Up counter Output as input to combinational circuit	combinational circuit output(similar to matrix2)
A B C D	**W X Y Z**
0 0 0 0	1 1 0 1
0 0 0 1	0 1 1 1
0 0 1 0	1 1 0 0
0 0 1 1	1 1 0 0
0 1 0 0	0 0 1 1
0 1 0 1	0 1 1 1
0 1 1 0	1 1 1 0
0 1 1 1	0 1 0 1
1 0 0 0	1 1 0 0
1 0 0 1	1 1 0 0
1 0 1 0	0 0 1 1
1 0 1 1	0 1 1 1

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1 1 0 0 1 1 0 1 1 1 1 0 1 1 1 1	1 1 1 0 0 1 0 1 0 0 1 1 0 1 1 1

The following are the equations for the combinational circuit obtained from the truth table.
W= AB'C'+AC'D'+A'B'C+A'CD'+A'B'D
X= A'C+AC'+D+A'B'
Y= A'C'D+BD'+AC
Z= BD+AC+A'C'
W, X, Y, Z are the outputs of the final circuit shown in the block diagram fig.1.

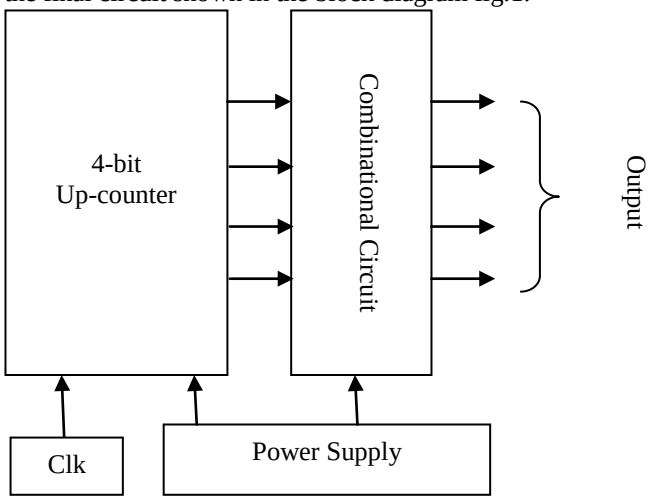

Fig.1: Block Diagram 4-bit synchronous counter

III. ADVANTAGES AND APPLICATIONS

The proposed method has the following advantages.

- Huge reduction in the area of data storage.
- Non-Volatile and Cheap.
- Corrupt free (free from virus attack).
- No data read problems like in CD/DVD due to scratches.
- Data extraction is simple and easy.
- Reduced data access time.

The following are the applications of the proposed data storage method.

- Used for storing any kind of digital information (Binary 1's and 0's) Ex. Data, Audio, Video etc.
- Can be used for corrupt free permanent storage of huge databases.

IV. ANALYSIS AND RESULTS

In the proposed data storage technique the percentage of hardware required for data storage gets reduced approximately by 90% that is $2^N * N$ Flip-flops get reduced to N-Flip-flops plus some combinational circuit. In this paper as an example a 4-bit synchronous counter is designed and implemented to count a needed sequence of matrix2 of Table-II successfully. Therefore similar design can be used for converting $2^N * N$ memory bits to a simple N-bit synchronous counter, which leads to the following results in Table-IV for different values of N.

Table-IV

Memory Size ($2^N * N$ memory bits)	Counter size (N-bit synchronous counter of needed sequence.)

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$2^4 * 4$ = 64-bits	4-bit
$2^8 * 8$ = 2048-bits	8-bit
$2^{16} * 16$= 1048576-bits	16-bit
$2^{32} * 32 = 137 * 10^9$ bits	32-bit

V. CONCLUSION

In this paper a new data storage technique is proposed and implemented successfully. The proposed technique can store large non-volatile corrupt free data in a simple N-bit counter in the form of its count, resulting in huge reduction of size, cost, and data access time.

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Author's Profile

MOHSIN KHAN A

He has received the B.E. degree in Telecommunication Engineering from Visveswaraya Technological University; Karnataka, India in 2006.He has completed M.Tech degree in Digital Electronics from Visveswaraya Technological University, Karnataka, India in 2011. He is now working as Assistant Professor in Department of Electronics & Communication Engineering, HMS Institute of Technology, Tumkur-572104, and Karnataka, India. His interest of research is in Analog and digital system design.

C P LATHA

She has received the B.E. degree in Instrumentation technology from Mysore University; Karnataka, India in 1991.She has completed M.E degree in Power Electronics from Bangalore University, Karnataka, India in 2000. Now she is pursuing PhD in wireless communication from Jain University. Presently working as Prof. .and Head in the department of Electronics & Communication Engineering, HMS Institute of Technology, Tumkur-572104, and Karnataka, India.

GHOUSE AHAMED Z

He has received the B.E. degree in Electronics & Communication Engineering from UBDT government college of Engineering, Kuvempu University; Karnataka, India in 2005.He has completed M.Tech degree in Digital Electronics from Visveswaraya Technological University, Karnataka, India in 2011. He is now working as Assistant Professor in Department of Electronics & Communication Engineering, HMS Institute of Technology, Tumkur-572104, and Karnataka, India. His interest of research is in Image processing.

FAZLULLA KHAN

He has received the B.E. degree in Electronics & Communication Engineering from Kuvempu University; Karnataka, India in 1996.He has completed M.Tech degree in Digital Electronics from Visveswaraya Technological University, Karnataka, India in 2011. He is now working as Assistant Professor in Department of Electronics & Communication Engineering, HMS Institute of Technology, Tumkur-572104, and Karnataka, India. His interest of research is in embedded system design and Real time systems.